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Development of 3-D Printed Hybrid Packaging for GaAs-MEMS Oscillators based on Piezoelectrically-Transduced ZnO-on-SOI Micromechanical Resonators

Di Lan
University of South Florida, dilan@mail.usf.edu

Development of 3-D Printed Hybrid Packaging for GaAs-MEMS Oscillators based on Piezoelectrically-Transduced ZnO-on-SOI Micromechanical Resonators

by

Di Lan

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Major Professor: Jing Wang, Ph.D.
Thomas M. Weller, Ph.D.
Arash Takshi, Ph.D.
Rasim Guldiken, Ph.D.
Shengqian Ma, Ph.D.

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DEDICATION

To my wife, my parents, my advisors, my friends

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ABSTRACT

Prior research focused on CMOS-MEMS integrated oscillator has been done using various foundry compatible integration techniques. In order to compensate the integration compatibility, MEMS resonators built on standard CMOS foundry process could not take full advantage of highest achievable quality factor on chip. System-in-package (SiP) and system-on-chip (SoC) is becoming the next generation of electronic packaging due to the need of multi-functional devices and multi-sensor systems, thus wafer level hybrid integration becomes the key to enable the full assembly of dissimilar devices. In this way, every active circuit and passive component can be individually optimized, so do the MEMS resonators and sustaining amplifier circuits. In this dissertation, GaAs-MEMS integrated oscillator in a hybrid packaging has been fully explored as an important functional block in the RF transceiver systems.

This dissertation first presents design, micro-fabrication, simulation, testing and modeling of ZnO piezoelectrically-transduced MEMS resonators. A newly designed rectangular plate with curved resonator body fabricated in-house exhibits a very high Q of more 6,000 in the air for its width-extensional mode resonance at 166 MHz. In addition, a rectangular plate resonator with multiple Phononic Crystal (PC) strip tethers shows low insertion loss of -11.5 dB at 473.9 MHz with a Q of 2722.5 in the air. An oscillator technology with high-Q MEMS resonator as its tank circuit is presented to validate its key functionality as a stable frequency reference across a wide spectrum of frequencies. Particularly, a piezoelectrically-transduced width-extensional mode MEMS resonator is strategically designed to operate at two distinct layout-defined mechanical modal frequencies (259.5MHz and 436.7MHz). These devices were characterized and modeled by

an extracted equivalent LCR circuit to facilitate the design of the oscillator using a standard circuit simulator. MEMS resonators have been integrated with the sustaining amplifier circuit at PCB level using wire-bonding technique and coaxial connectors. As shown by the time-domain measurements and frequency-domain measurements, these oscillators are capable of selectively locking into the resonance frequency of the tank circuit and generating a stable sinusoidal waveform. Meanwhile, the phase noise performance is rigorously investigated within a few oscillator designs. At last, 3-D printed hybrid packaging using additive manufacturing and laser machining technique has been developed for integrating a MEMS resonator on a silicon-on-insulator (SOI) substrate and a GaAs sustaining amplifier. Fabrication process and fundamental characterization of this hybrid packaging has been demonstrated. On-wafer probe measurements of a 50 Ω microstrip line on ABS substrate exhibit its insertion loss of 0.028 dB/mm at 5 GHz, 0.187 dB/mm at 20 GHz and 0.512 dB/mm at 30 GHz, and show satisfactory input and output return loss with the 3-D printed package. Parylene N is also experimentally coated on the package for improving water resistance as a form of hermetic packaging.

CHAPTER 1: INTRODUCTION

1.1 Overview

Due to an explosive growth of personal mobile devices and ever-growing demand of multifunctional gadgets in the wireless communications, a great amount of research effort has been devoted to making present and future RF systems with lower size, weight, and power (SWaP) along with enriched functionalities and higher performance.

As a key enabler of the evolution of integrated wireless systems, Si CMOS technology continues to progress toward increasing functionality and complexity predicted by Moore's law with lower size, weight, and power (SWaP). Meanwhile, compound semiconductor III-V transistor devices and circuits have revolutionized RF electronics by offering superior frequency, gain, noise, and power characteristics at microwave and millimeter wave frequencies.

Despite the continuous success of the ever-growing IC industry fueled by Moore's law, the dependency on high quality factor on-chip passives is the key limiting factors against system-level miniaturization and integration. With the rapid development of MEMS technology for the past decade, it is now becoming a viable solution to batch-produce high-performance RF passive components, such as tunable filters, switches, capacitors, inductors and high-Q resonators for the next generation of wireless communication systems. Therefore, a convenient and parasitic-free heterogeneous integration of MEMS passives and III-V or Si CMOS transistor devices is required to create miniaturized, high-performance RF front-ends.

In modern wireless communications, an oscillator is an essential component of any wireless transceivers to provide performance-setting frequency references with high precision and low

noise. Traditionally, off-chip quartz crystal oscillators have been the most widely accepted choice despite its low level of integration with IC's and limited frequency range up to 100MHz. The advent of high-Q MEMS resonators has enabled the on-chip MEMS-based oscillators that can be fully integrated with on-chip transistor circuits, such as sustaining amplifiers, thus exhibiting a promising low phase noise at much higher frequencies than that of the quartz crystals.

Prior research towards development of on-chip frequency-setting passives has been focused on piezoelectrically-transduced contour-mode MEMS resonators, which do not require a polarization or bias voltage to operate and exhibit characteristic motional resistance typically lower than 1 kΩ. These two highly-unique advantages make the piezoelectrically-transduced contour-mode MEMS resonators a very promising alternative for implementation of oscillators at gigahertz frequencies.

Wafer level packaging is a promising solution for system-in-package (SiP) level of implementation of RF front end modules. In this work, seamless integration of high-Q MEMS resonator (array) and monolithic microwave integrated circuit through 3-D printed hybrid package using additive manufacturing and laser machining is going to be investigated to fulfill the stringent performance requirements for fully integrated reference oscillators.

1.2 Review of MEMS Integration

1.2.1 CMOS-MEMS Integration

Si CMOS as the most popular and promising technology exists inside every electronic device in our life. The recent advances in MEMS technology have become a promising enabler to yield RF modules and sub-systems with new functions. Consequently, RF MEMS devices have been successfully integrated with CMOS process with traditional hybrid approaches or advanced monolithic approach using similar or process compatible materials.

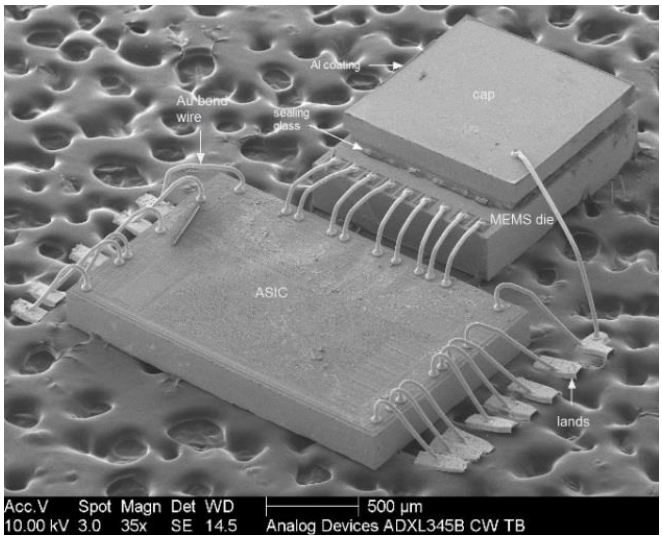


Figure 1.1 – A SEM image of a MEMS die wirebonded to a CMOS chip through a hybrid modular integration

The hybrid approaches of CMOS-MEMS integration as shown in Figure 1.1 are typically utilized by chip to wafer bonding (C2W), wafer to wafer bonding (W2W) and any other wafer stacking techniques [1]. This modular packaging method not only facilitates parallel work on individual design and optimization of MEMS devices and CMOS circuits, but also allows the maximum design freedom of MEMS and CMOS components. Therefore, hybrid approach has been widely employed on various products till today [2-4].

On the other hand, the monolithic approach has its key features against the hybrid approach, which are further miniaturization ability, low cost from single chip manufacturing and testing, and enhancement of signal to noise ratio due to parasitic reduction from shorter interconnects and its higher level of integration.

Within a single chip CMOS-MEMS development, monolithic integration can be realized through four main approaches: the pre-CMOS technology shown in Figure 1.2 (a); the intra-CMOS approach shown in Figure 1.2 (b); the post-CMOS technology shown in Figure 1.2 (c); and post-processing of CMOS-back end of line layers (BEOL) approach shown in Figure 1.2 (d) [5-8]. In

addition to great amount of integration development efforts required by all four monolithic approaches, they encounter different fabrication limitations and constraints such as MEMS layer thickness, thermal budget, and so on.

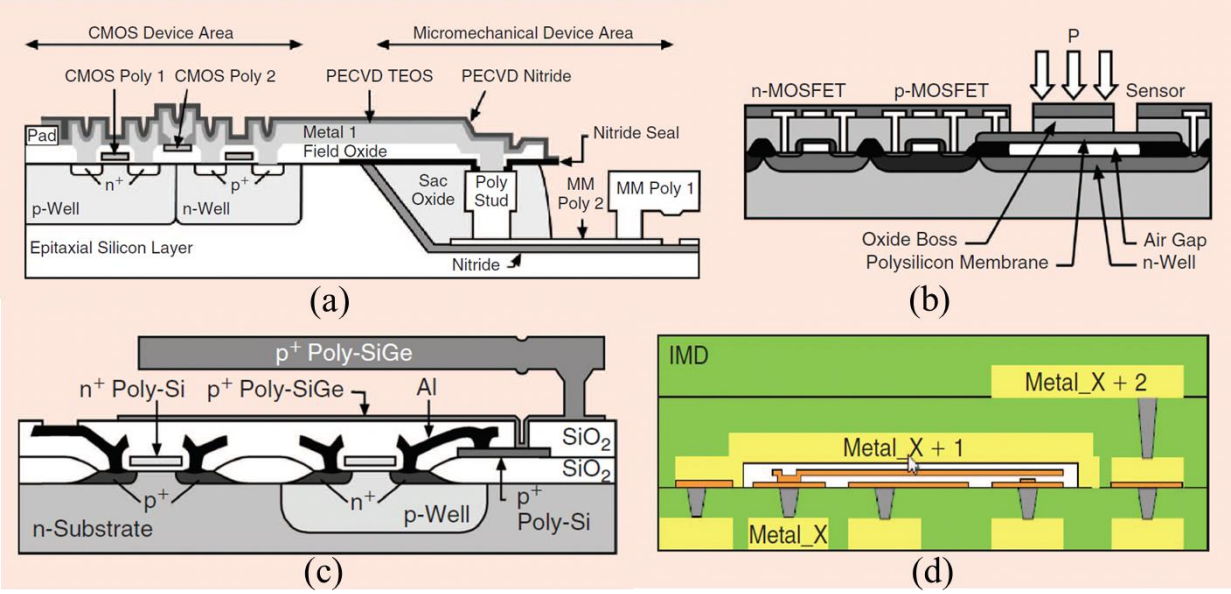


Figure 1.2 – Cross-sectional schematic diagrams of (a) an integrated CMOS-MEMS chip illustrating the well-known approach by Sandia National Lab [9]; (b) Infineon Technologies' integrated MEMS technology for the fabrication of pressure sensors [10]; (c) poly-SiGe microstructure fabricated by post-CMOS surface micromachining techniques on top of a completed CMOS substrate wafer [11]; and (d) a Nanomech MEMS embedded in the CMOS back end [12]

1.2.2 Wafer Level Packaging (WLP) and System in Package (SiP)

With the increasing demand for the miniaturized packages of multi-dies and multi-sensor devices in the high end electronics, wafer level packaging has been introduced as an innovative solution to accommodate all the manufacturing requirements. The main driving force, in terms of the performance metrics, for wafer level packaging is illustrated in Figure 1.3.

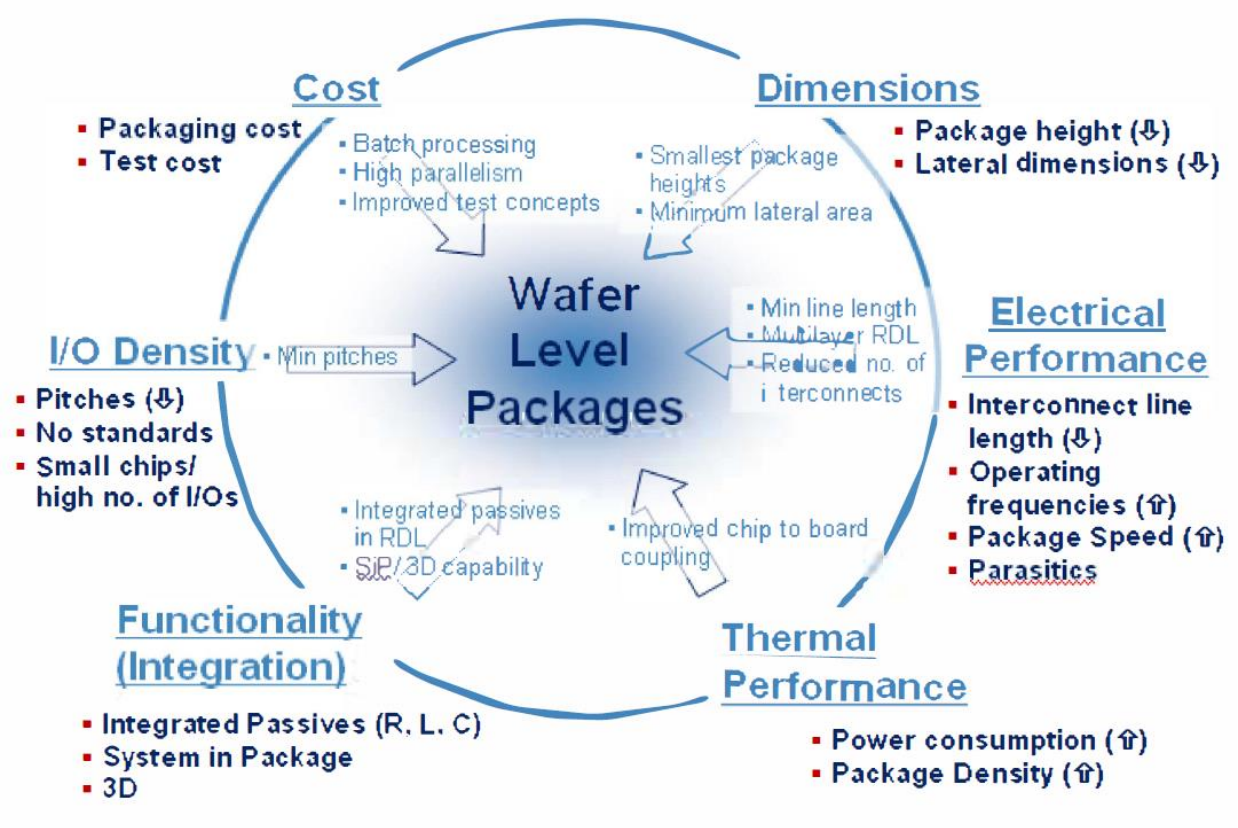


Figure 1.3 – Driving force for wafer level packaging [13]

Since "Fan-in" WLP as shown in Figure 1.4 (a) is typically limited to be less than 6mm x 6 mm in order to pass board level reliability requirements, "Fan-out" WLP has been invented for higher ball counts WLP and developed by extending the package area beyond the chip size as shown in in Figure 1.4 (b) [13]. Embedded wafer level ball grid array (eWLB) as the most prominent type of FO-WLP current available in industry was demonstrated by Infineon Technologies in 2008 [14]. The eWLB process starts with embedding a singulated die into an artificial wafer using a wafer level molding technique. And then metallization and isolation are applied on the die surface to fan-out the interconnections to the outside solder balls by standard wafer level lithography and patterning technique.

For side by side multichip eWLB packaging, additional number of interconnections between dies and dies to solder balls is significantly increased. Thus, redistribution layer (RDL) is

needed since it does not only yield higher performance electrical connection and complex routing using thin film technology, but also can provide embedded passive components using a multi-layer structure. Comparing to traditional wire bonding, RDL has fine pitch metallization and well-controlled interconnection with less parasitic. Low loss tall microstrip transmission lines (TMLs) in eWLB is fabricated and reported with insertion loss of 0.1 dB/mm @ 10GHz and 0.25 dB/mm @ 60GHz [15].

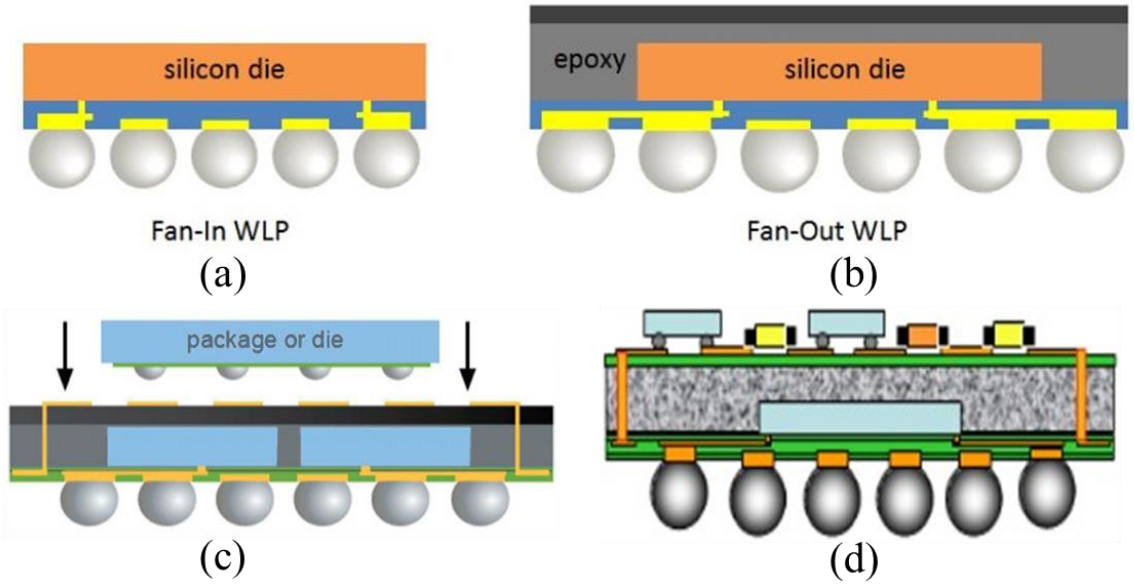


Figure 1.4 – Conceptual schematic diagrams illustrating (a) eWLB (FI-WLP); (b) eWLB (FO-WLP); (c) Package-on-package (PoP) using double-side eWLB packaging [13]; and (d) System-on-Wafer (SoW) using double-side eWLB packaging [16]

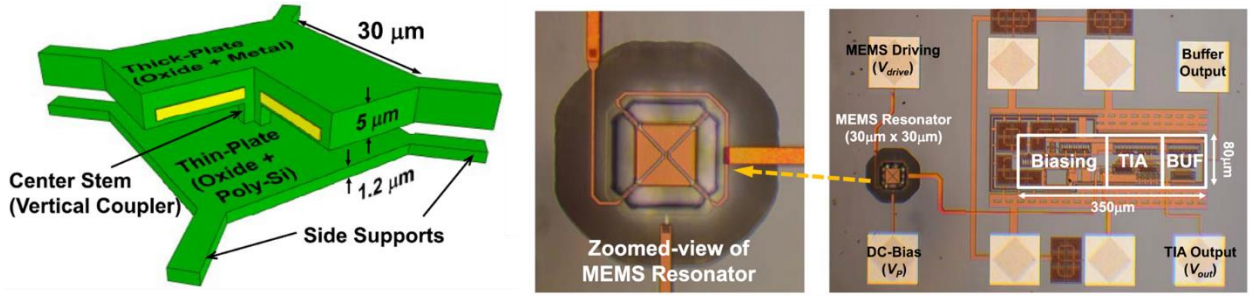
As eWLB applications are expanding to logic ICs, MEMS, III-V devices and discrete RF integration, 3-D eWLB approach such as PoP shown in Figure 1.4 (c) and SoW shown in Figure 1.4 (d) is critically needed for the miniaturization at sub-system and system level. It is gradually becoming a mainstream technology because of its flexibility of combining dissimilar materials and various technologies. However, due to the fact that 3-D eWLB is relied on through silicon vias (TSVs) to vertically connect the stacking chips, the quality of TSVs, which directly affects the

performance of the entire integration, is required to be fully characterized. Future study and research of interconnection and wiring are needed as well.

1.3 Current State of the Art MEMS-Based Oscillators

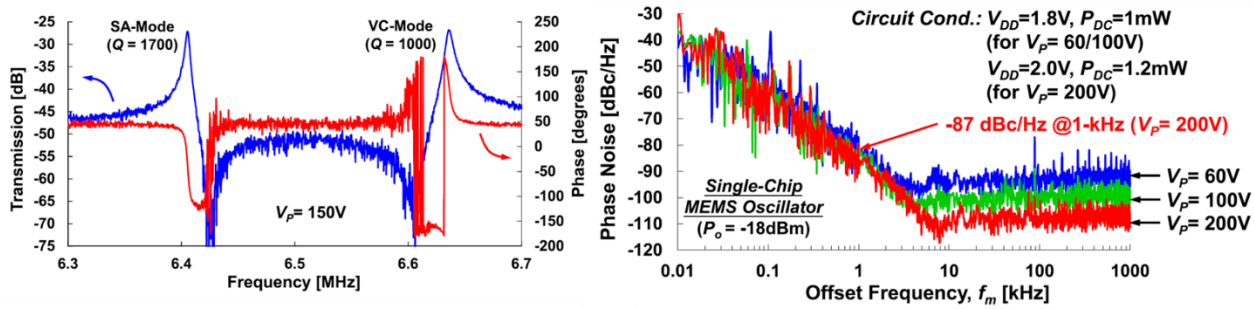
1.3.1 Monolithic CMOS-MEMS Oscillators

Several fully monolithic MEMS-CMOS oscillators have been successfully demonstrated using process compatible materials with mature and well-developed complimentary metal-oxide-semiconductor (CMOS) foundry process. CMOS-MEMS vertically-coupled resonator and their associated on-chip transimpedance amplifiers in Figure 1.5 (b) are fabricated utilizing a standard TSMC 0.35 μm CMOS technology from Sheng-Shian Li's group in 2015 [17]. This MEMS resonator shown in Figure 1.5 (a) consists of patterned metal electrodes (yellow) embedded inside the top thick oxide plate (green), bottom thin plate formed by polysilicon and oxide polysilicon and an oxide stem placed at the center. There are two vibration modes, which are saddle (SA) mode and vertically-coupled (VC) mode in this resonator. Because of the large capacitive transduction gap (>1 μm) from the 0.35 μm CMOS process, A DC bias voltage (~200 V) is required to actuate the resonator with the resultant motional resistance of 60 kΩ. Transmission response of the resonator plotted in Figure 1.6 (a) shows 6.5 MHz resonant frequency, 1,000 quality factor in vacuum (< 0.1 mTorr) for VC-Mode under 150 V DC biasing condition. Comparing to other prior reports of monolithically integrated oscillators [18-20], the best-case phase noise of the VC-mode oscillator shown in Figure 1.6 (b) with −97 dBc/Hz at 1-kHz and −118 dBc/Hz at 1-MHz offset from carrier respectively is slightly better.



(a) (b)

Figure 1.5 – (a) Perspective view of the vertically-coupled resonator; (b) Optical photos of the CMOS-MEMS resonator oscillator [17]



(a) (b)

Figure 1.6 – (a) Magnitude and phase responses of the proposed resonator; (b) Phase noise performance comparison [17]

Another monolithic CMOS-MEMS oscillator shown in Figure 1.7 (a) using TSMC 0.35 μm CMOS technology has also been reported in the same group [21]. The CMOS-MEMS resonator was released using chip level post-CMOS process without a mask layer. The resonator was characterized to have 700 kΩ motional resistance (R_M) and quality factor up to 3,000 under a vacuum level of 100 μTorr environment while biasing with 45 V. The quality factor (Q) of such resonator dramatically degrades to only 150 once it is operated under ambient pressure. Due to the extremely high R_M, a 4-stage transimpedance amplifier is designed in Figure 1.7 (b) to provide enough gain and bandwidth to sustain the oscillation at 1.2 MHz. The output spectrum of the oscillator is plotted in Figure 1.8 (a). While only consuming less than 1.3 Mw of power, this

monolithic CMOS-MEMS oscillator exhibits measured phase noise of −112 dBc/Hz at 1-kHz offset from the carrier, and −120 dBc/Hz at 1-MHz offset from carrier as shown in Figure 1.8 (b).

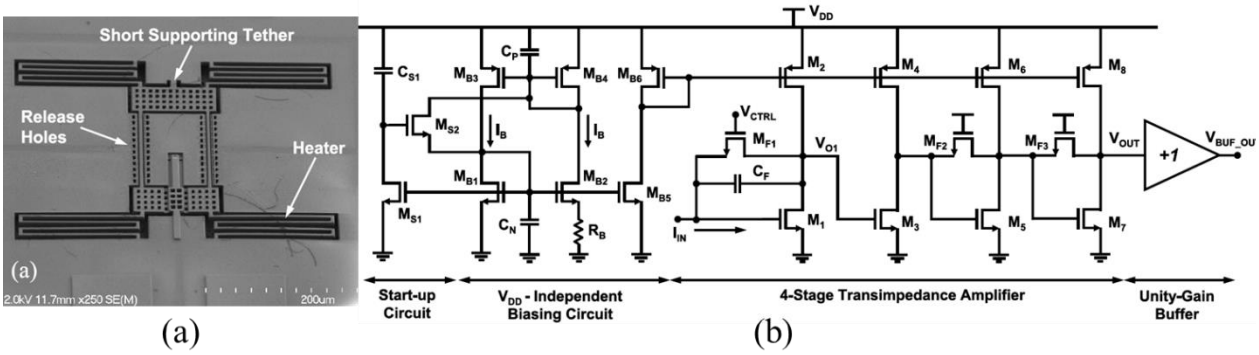


Figure 1.7 – (a) A SEM image of the CMOS-MEMS resonator; b) schematic of a 4-stage transimpedance amplifier (TIA) with independent biasing circuit [21]

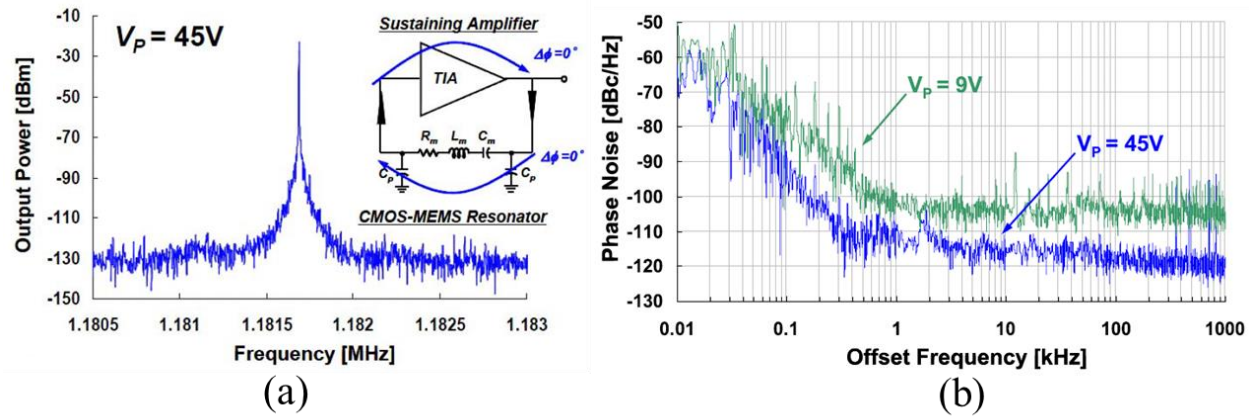


Figure 1.8 – (a) Output spectrum of the CMOS-MEMS oscillator; (b) phase noise performance of the CMOS-MEMS oscillator under two different biasing voltages of the resonator [21]

1.3.2 Piezoelectric AlN-Based CMOS Oscillators

In Piazza's group, they have done research on AlN Contour-Mode MEMS resonator based CMOS oscillators for years, especially focusing on reconfigurable CMOS oscillators for generation of multiple frequencies recently [22]. Four resonators with a quality factor of 1,750 to 3,000 are designed based on four sets of parameters, which are width, finger number, length and

AlN thickness, therefore resonance frequencies of 268 MHz, 483 MHz, 690 MHz and 785 MHz are generated from these oscillator tanks. AlN resonators, CMOS switches and COMS amplifiers using 0.5 μm technology are integrated together on a printed circuit board (PCB) through wirebonding as shown in Figure 1.9 (a). Phase noise performance for these oscillators at the different frequency is plotted in Figure 1.9 (b) and the best one achieves -95 dBc/Hz at 1-kHz offset from carrier, and −160 dBc/Hz at 1-MHz.

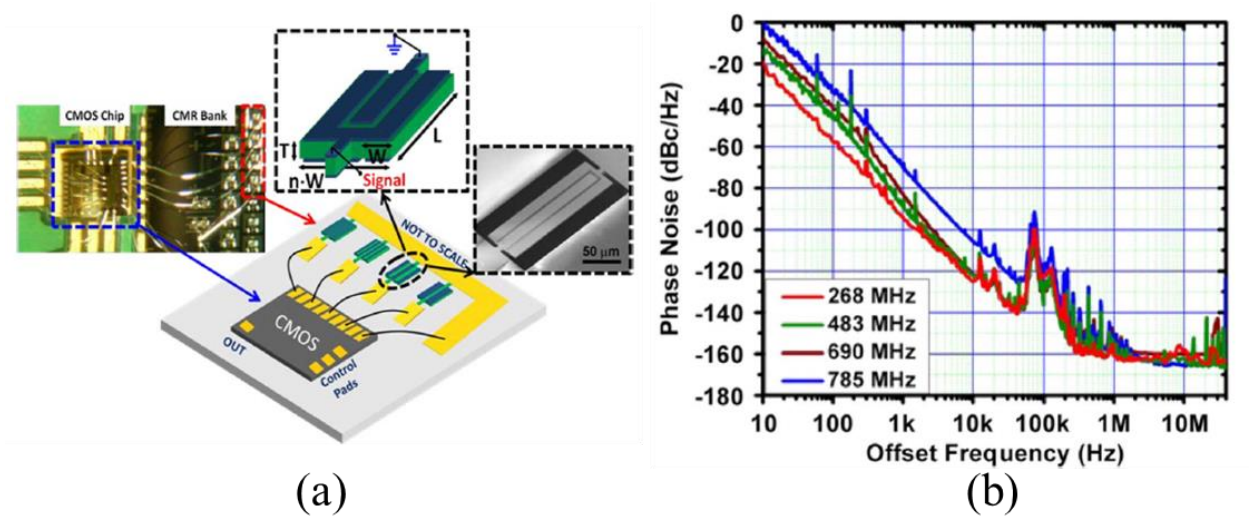


Figure 1.9 – (a) Overview of the reconfigurable CMOS oscillator on prototype based on four-different-frequency AlN MEMS resonators, and scanning-electron-microscope (SEM) of the resonator; (b) phase noise performance of the reconfigurable CMOS oscillator

Instead of using multiple resonator tank for various frequency references, a single AlN-on-Si MEMS oscillator has also been demonstrated under its dual-frequency operation using first/third (35.5/105.7 MHz) order modes of the MEMS resonator [23]. A switching network circuit is incorporated into transimpedance amplifier circuit design so that the oscillation frequency changes with different phase shift. The measured phase noise for both frequencies is around -110 dBc/Hz at 1 kHz offset from carrier and -140 dBc/Hz 1MHz offset from carrier.

1.3.3 MEMS-Based GaN Oscillators

Recently, a 1 GHz monolithically integrated GaN-MMIC oscillator shown in Figure 1.10 (a) has been realized using GaN-on Si heterostructure from Raytheon [24]. The Lamb mode GaN resonator is side by side with the rest of circuits and released from a deep trench etch followed by a silicon etch as shown in Figure 1.10 (b). Fabricated resonator has 390Ω motional resistance and a quality factor of 4,250 while it is measured under a vacuum level of 10^{-5} Bar. The phase noise performance of this GaN-MEMS oscillator exhibits phase noise of -82 dBc/Hz at 1 kHz offset from carrier and -130 dBc/Hz 1MHz offset from carrier. This oscillator only occupied 268 x 214 μm^2 area on the chip which is 10 times smaller than the FBAR oscillator [25].

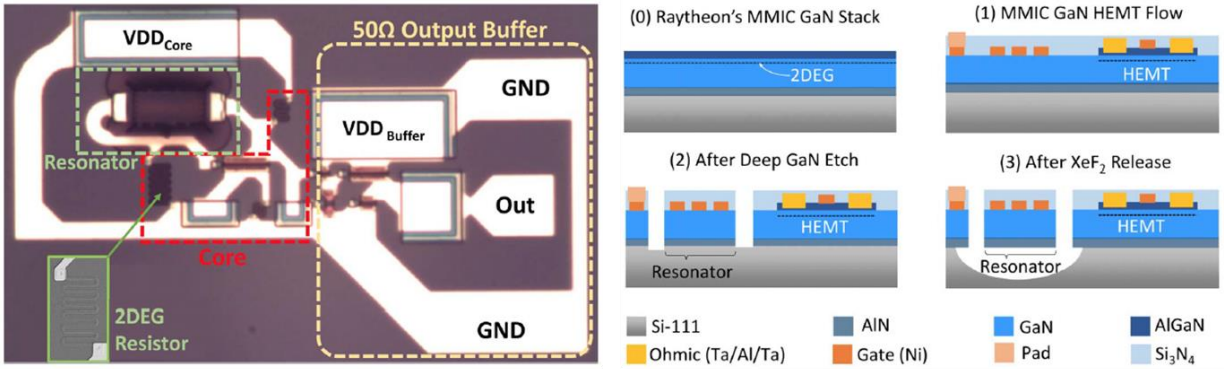


Figure 1.10 – (a) Overview of the GaN-MEMS oscillator; (b) an Au-free modified MMIC HEMT process for GaN-MEMS resonators [24]

1.3.4 Drawbacks of the Current State-of-the-Art Technology

- Despite the fact that MEMS resonator fabricated with CMOS compatible technology is monolithically integrated to the rest of the circuit, the oscillator is still required to operate under vacuum condition while exhibiting low oscillation frequency. Due to the extremely high motional resistance of the CMOS-MEMS resonator even at relatively low frequencies, very complex performance-demanding multi-stage transimpedance amplifier circuit design is often required which causes longer design cycle and a bit higher power consumption.

- AlN resonator exhibits high resonance frequency and reasonable quality factor of less than 3,000 in air. However, wirebonded oscillator not only limits the best achievable performance but also hinders future miniaturization.
- Although newly developed GaN-MEMS oscillator has decent performance and tiny size because of its monolithic integration, it still requires vacuum level package and highly specialized GaN process. After all, GaN does not offer comparable piezoelectric coefficient on par with that of AlN, ZnO, etc.

1.4 Dissertation Organization

This dissertation is organized into six chapters and three appendices. Chapter 1, as an introductory chapter, first presents an overview and motivation of this dissertation work. And then it focus on reviewing current MEMS integration technology and current state of the art MEMS based oscillator design. The main goals and contributions of this dissertation are also described at the end of this chapter.

In Chapter 2, fundamental knowledge and basic mathematic formula of piezoelectricity are provided. In addition, this chapter presents the equivalent mechanical domain and electrical domain representation of a MEMS resonator, especially Butterworth-Van Dyke (BVD) circuit model as an extended analysis of the electrical model. Detailed fabrication processes for ZnO piezoelectric MEMS resonators on Silicon-on-insulator and Diamond-on-Silicon wafer are described in Chapter 3, followed by the comparison between measured and simulated results of micro-fabricated devices. Substrate model including probe pad and microstrip line is analyzed and discussed in this chapter as well. Chapter 4 presents the design and implementation of MEMS based oscillators using a ZnO piezoelectric resonators using different transistor technology and fabrication methods. In Chapter 5, a novel 3-D hybrid package using additive manufacturing and

laser machining is introduced and the fabrication process is described in detail. The integration of multiple ICs on a 3-D printed substrate is demonstrated along with the analysis of its performance.

Chapter 6 concludes the findings of this work while also providing the viable directions for future research work.

1.5 Contributions

In this work, ZnO piezoelectrically-transduced resonators have been designed, fabricated and demonstrated with high-Q and high-frequency that is one of the main contributions of this dissertation work. The layout for the 5-mask fabrication process is drawn via CAD tool. Various designs (e.g., curved resonator body, Phononic Crystal strip tethers, and acoustic reflector) of the width-extensional mode resonators are designed for high-Q and low insertion loss devices. Proposed fabrication processes for the resonator on SOI and diamond-on-silicon (DOS) have been successfully implemented at the cleanroom facility at USF. Those micro-fabricated resonators are intensively characterized through measurement and simulation. Suitable ones are selected as resonator tanks for the oscillator design.

To facilitate the oscillator design and circuit analysis for a complete reference oscillator circuit simulation, electrical equivalent circuit model of the piezoelectrically-transduced resonator has been developed and experimentally verified. Measured frequency response of the resonator are compared with simulation results for additional validation. The sustaining amplifier circuits are designed based on the characteristics of the fabricated resonators for the oscillator design. MEMS resonators operating at 260 MHz and 430 MHz are integrated with the sustaining amplifier circuit using wire-bonding technique and coaxial connectors. Thus, the second main contribution is the implementation of a dual-frequency MEMS based oscillator using a single ZnO-on-SOI

resonator which is published in [57]. The phase noise performance for those oscillators have been rigorously measured and analyzed, which is largely on par with those of the prior works.

Gallium arsenide (GaAs) high-electron-mobility-transistor (HEMT) is one of the III-V direct bandgap semiconductor technologies that allows the monolithic integrated circuits (MMIC) to operate at very high frequencies with low noise figure, due to its high electron mobility and excellent noise parameters. Superior properties of GaAs make it widely used in microwave and RF circuities, and an excellent candidate for oscillator circuit using in RF systems. Hence, the sustaining amplifiers for oscillator design using the GaAs HEMT technology have been designed and implemented for the future chip-level integration. To further understand GaAs HEMT technology from the complementary foundry service from TriQuint Semiconductor Inc., a 2-22 GHz distributed low-noise amplifier (LNA) is designed and taped out as the third main contribution. The S-parameters of the LNA along with its noise figure are measured and compared with the simulation results. Also, this chip is used for development of the hybrid package.

The primary goal of this work is to develop a generic hybrid integration methodology for a MEMS resonator and GaAs MMIC to offer ease of manufacturing, individual optimization of circuitries, reduction of design cycle, and low-level parastics along with a better SWaP. Therefore, 3-D printed interconnects and hybrid package for integration of multiple IC chips using additive manufacturing and laser machining have been successfully developed and demonstrated for the first time.

CHAPTER 2: BACKGROUND

2.1 Piezoelectric Effect

Piezoelectric effect was first discovered by Pierre and Jacques Curie in 1881. They demonstrated that mechanical stresses from external pressure in certain materials such as topaz, zinc blende, and quartz can generate electric charges. Piezoelectric effect describes a link between electrostatics and mechanics and it is normally understood as the linear electromechanical interaction between the mechanical and the electrical state in crystalline materials with no inversion symmetry [26]. The piezoelectric effect can be simply explained by a molecular model shown in Figure 2.1. In Figure 2.1 (a), a molecule that has 3 negative and positive charges is electrically neutral without subjecting an external force. However, when the molecule is deformed with an external mechanical stress as shown in Figure 2.1 (b), a dipole is created by the separation of the positive and negative around the center position. As a result, the positive and negative charges facing each other inside the material are canceled and then the material is polarized with the fixed charges on the surface shown in Figure 2.1(c). This phenomenon is called direct piezoelectric effect. Piezoelectric materials can generate and accumulate an electrical charge from an applied mechanical force. The amount of charge generated is directly proportional to the applied mechanical stress strength. Vice versa, a reverse piezoelectric effect also exists because piezoelectricity is a reversible and bi-directional energy conversion mechanism. A mechanical deformation results in a piezoelectric material when an electrical field is applied.

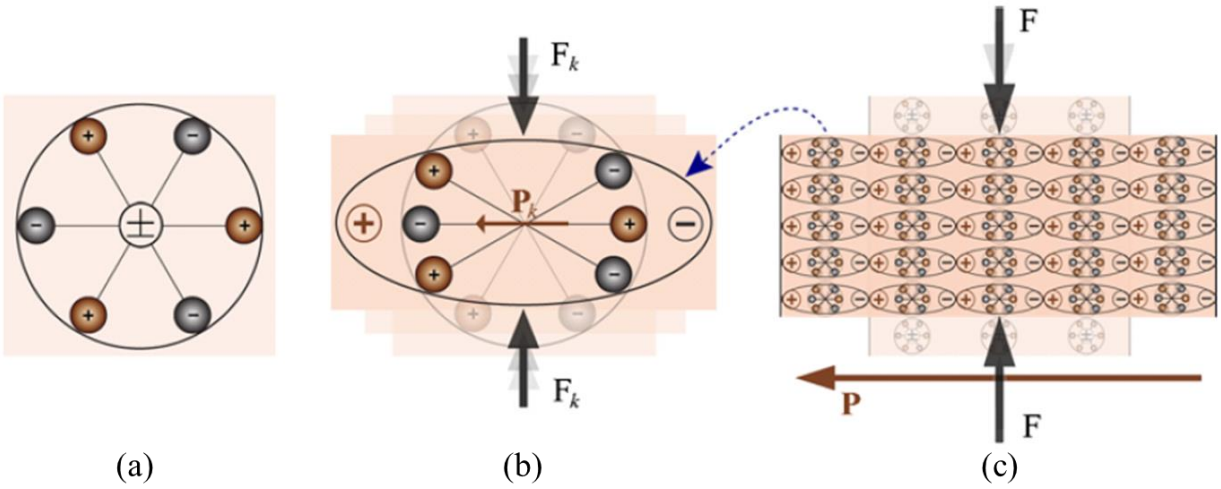


Figure 2.1 – A simple molecular model of piezoelectric effect: (a) an unperturbed molecule with no piezoelectric polarization (though prior electric polarization may exist); (b) The molecule subjected to an external force (F_k), resulting into polarization (P_k) as indicated; (c) The polarizing effect on the surface when piezoelectric material is subjected to an external force [27]

2.2 Mathematical Formation for Piezoelectric Effect

The piezoelectric effect in practice results in a cross-coupling between the electrical and mechanical behavior of a material. Since piezoelectric materials are anisotropic, their physical properties (e.g., permittivity, elasticity, and piezoelectric constant) are tensor quantities. Base on the linear theory of piezoelectricity [28], the equations that describe the relationship between mechanical stress (T), mechanical strain (S), an electrical field (E) and electrical displacement (D) are given as:

$$S_P = s_{pq}^E T_q + d_{pk} E_k \tag{2.1}$$

$$D_i = d_{iq} T_q + \varepsilon_{ik}^T E_k \tag{2.2}$$

where S_p is the mechanical strain in the p direction, $s_{pq}{}^E$ is elastic compliance under constant electric field, T_q is mechanical stress in the q direction, d_{kp} is piezoelectric constant, E_k is the electric field in the k direction, $\varepsilon_{ik}{}^T$ is dielectric constant tensor under constant stress, and D_i is electric displacement in the i direction. Those constants are expressed with two subscript indices.

The first subscript index defines the axis of the excitation and the second one refer to the actuation orientation.

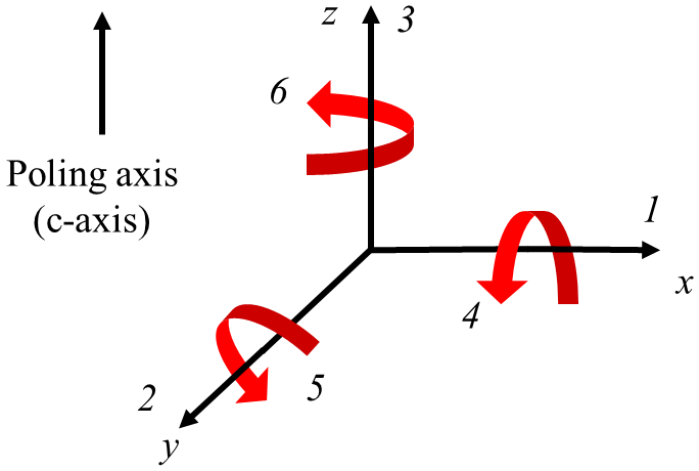


Figure 2.2 – Tensor directions for defining piezoelectricity

The crystallographic axes depicted in Figure 2.2 are defined using the notation of a Cartesian rectangular system. Original directions of x, y, and z are represented by 1, 2, and 3, respectively, whereas the shear planes are labeled as 4, 5, and 6, respectively. Usually, the direction of positive polarization is chosen to coincide with the z-axis.

Four alternate forms explain the electromechanical coupling from different perspectives are listed below.

The stress-charge form is expressed as:

$$T_{6\times1} = c^{E}_{6\times6} \cdot S_{6\times1} + e_{6\times3} \cdot E_{3\times1}$$
$$D_{3\times1} = e_{3\times6} \cdot S_{6\times1} + \varepsilon^{S}_{3\times3} \cdot E_{3\times1} \quad (2.3)$$

The strain-charge form is expressed as:

$$S_{6\times1} = s^{E}_{6\times6} \cdot T_{6\times1} + d_{6\times3} \cdot E_{3\times1}$$
$$D_{3\times1} = d_{3\times6} \cdot T_{6\times1} + \varepsilon^{T}_{3\times3} \cdot E_{3\times1} \quad (2.4)$$

The strain-voltage form is expressed as:

$$S_{6\times1} = s^{D}_{6\times6} \cdot T_{6\times1} + g_{6\times3} \cdot D_{3\times1}$$
$$E_{3\times1} = -g_{3\times6} \cdot T_{6\times1} + \beta^{T}_{3\times3} \cdot D_{3\times1} \quad (2.5)$$

The stress-voltage form is expressed as:

$$T_{6\times1} = c^{D}_{6\times6} \cdot S_{6\times1} - h_{6\times3} \cdot D_{3\times1}$$
$$E_{3\times1} = -h_{3\times6} \cdot S_{6\times1} - \beta^{S}_{3\times3} \cdot D_{3\times1} \quad (2.6)$$

where *c* is the stiffness matrix and *e* is the piezoelectric constant matrix. β is the inverse matrix of permittivity, and *d*, *g*, and *h* are the alternate forms of piezoelectric constants.

2.3 Piezoelectric Materials

Piezoelectric crystals and piezoelectric ceramics are two major categories of piezoelectric materials. Quartz as the most well-known piezoelectric material is a natural piezoelectric crystal that is widely used in piezoelectric filters, timing and frequency reference devices such as oscillators for a few decades because of its mechanical strength, small dielectric loss, chemically stability and low thermal coefficient expansion, which translates to an excellent dimensional stability under temperature variations. Although it has such desirable characteristics, the practical frequency limitation for a fundamental mode AT-cut crystal is around 30 MHz [29].

Meanwhile, there are several also excellent ceramic materials that exhibit piezoelectric behavior and are most widely used in transducers and MEMS applications such as aluminum nitride (AlN), zinc oxide (ZnO), barium titanate ($BaTiO_3$) and lead-zirconate-titanate (PZT). Although $BaTiO_3$ has a very high piezoelectric strain coefficient d_{31} of -58 which is more than 10 times higher than AlN and ZnO, its high thermal expansion coefficient and low Curie point limit itself for further development. Similar to $BaTiO_3$, PZT also has extremely high electromechanical coupling coefficient. However, process compatibility of PZT prevents itself from being widely

used with many CMOS technologies due to the fact PZT contains the lead element. Since high-quality AlN and ZnO films can be easily obtained by sputtering at a relatively low temperature (below 400 °C) to offer compatibility with CMOS processing, AlN and ZnO become the most widely used piezoelectric thin film material in MEMS applications. Furthermore, the low processing temperatures of these materials also enable post-CMOS integration process while retaining aluminum as the metallization layer. Table 2.1 summarizes the properties of these materials mentioned above.

Table 2.1 – Properties of the most commonly used piezoelectric materials [30-32]

Material Properties	Symbol	Unit	AIN	PZT	ZnO
Elastic Modulus	E	GPa	330	53	123
Density	ρ	kg /m^3	3260	7600	5676
Acoustic Velocity	υ	m/s	10400	3300	4655
Poisson Ratio	σ		0.24	0.25-0.31	0.18-0.36
Piezoelectric Strain Coefficient	d_{31}	pC /N	-2	-123	-5
Piezoelectric Strain Coefficient	d_{33}	pC /N	5	289	12.4
Piezoelectric Strain Coefficient	d_{15}	pC /N	3.6	495	-8.3
Relative Permittivity	ε_r		8-10	400-1900	9-11
Electrical Resistivity	ρ_e	Ω cm	10^{10}-10^{14}	10^7-10^9	10^8-10^9

AlN film has several advantages over ZnO film, which make it widely used for commercial applications. AlN film is totally compatible with semiconductor technology. However, ZnO can be problematic with process contamination issues because Zn is a fast diffusing ion. Moreover, AlN intrinsically has a large band gap of 6 eV along with a large resistivity. On the contrary, it is

more difficult to obtain a high resistivity for ZnO film because of its low band gap. Nonetheless, more MEMS researchers in academia have been conducted with ZnO than AlN due to the ease of sputtering ZnO films using the lab-scale sputtering equipment.

2.4 Piezoelectrically-Transduced MEMS Resonator and Vibrational Modes

A thin-film piezoelectric-on-substrate (TPoS) resonator shown in Figure 2.3 consists of a thin-film piezoelectric layer embedded between two metallic electrode layers and a relatively thick substrate structural layer. The structural layer usually comprises a large portion of the resonant structure and it is typically chosen from a low acoustic loss material such as single crystal silicon. In this design, when an AC electric field is applied across the piezoelectric film between the top and bottom electrode layers at the natural resonance frequency of the substrate structure material, the thin-film piezoelectric layer is excited into its resonance mode. The applied electrical field across the piezo-film will drive the resonator body to expand and contract through the converse piezoelectric effect. In return, deformation from such resonance mode induces periodic piezoelectric charges on the surface of the output electrode layer thus producing a motional current.

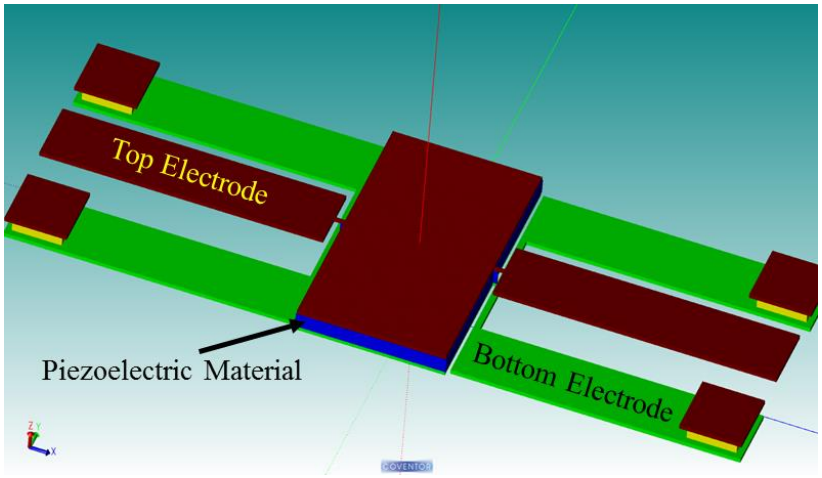


Figure 2.3 – 3-D view of a rectangular plate piezoelectric resonator

Analysis of different excitation and vibration modes of this acoustic resonator is carried out using the constitutive equations studied in the previous section. Depending on the particular

piezoelectric coefficient that is used to excite the plate into resonance, the device with rectangular plate can be actuated in four modes: Thickness excitation of the thickness vibration ("33" longitudinal mode); Thickness excitation of the extensional vibration ("31" flexural mode); Thickness excitation of the transversal vibration ("31" shear mode); Lateral excitation of the shear-mode vibration ("15" shear mode). Figure 2.4 illustrates the vibration modes for piezoelectric resonators mention above.

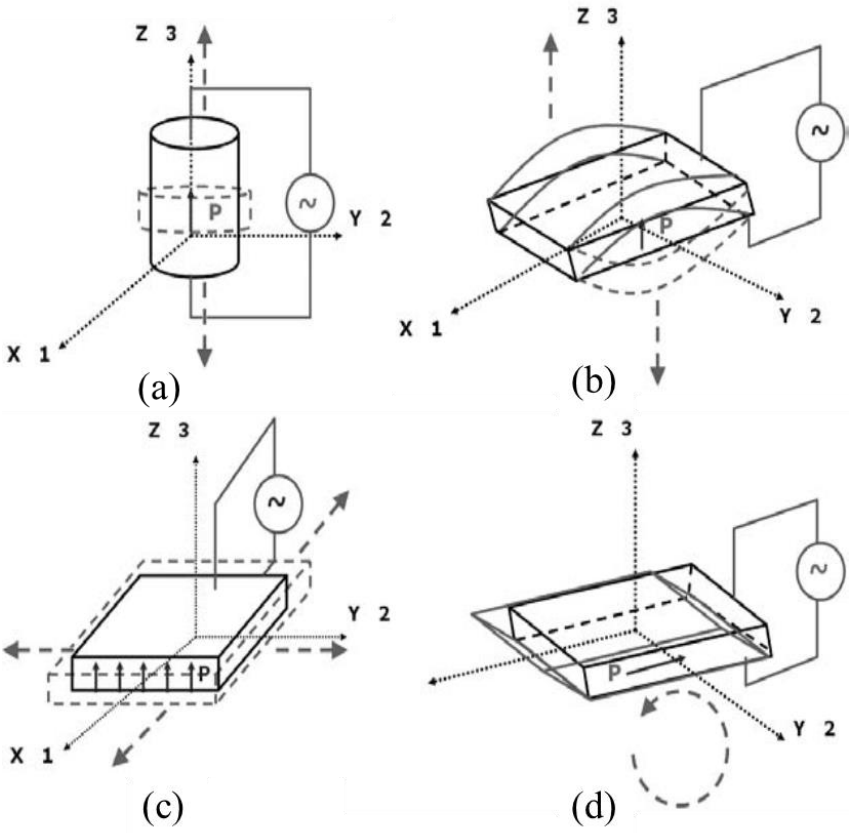


Figure 2.4 – Vibration modes of TPoS resonators: (a) longitudinal ("33" mode); (b) extensional ("31" mode); (c) thickness-transversal ("31" shear mode); and (d) lateral-shear ("15" mode) [33]

Thickness-mode is employed in AlN Thin-Film Bulk Acoustic Resonators (FBAR) and the fundamental resonance frequency is set by the film thickness, therefore allowing one operation frequency on a single substrate. The electric field applied on FBAR is along the z-axis ("3")

direction, thus and the crystal will experience strain or stress in the preferred crystal orientation ("3"). For resonators operating in shear-modes, the electrical field must be applied perpendicular to edges of the plate in order to drive the structure in resonance. The resonance frequency of a contour-mode is determined by the lateral dimension of the plate. The dimensions of the plate can be precisely defined by the device CAD layout, facilitating the design and fabrication of this kind of structures to achieve multiple resonance frequencies on a single chip.

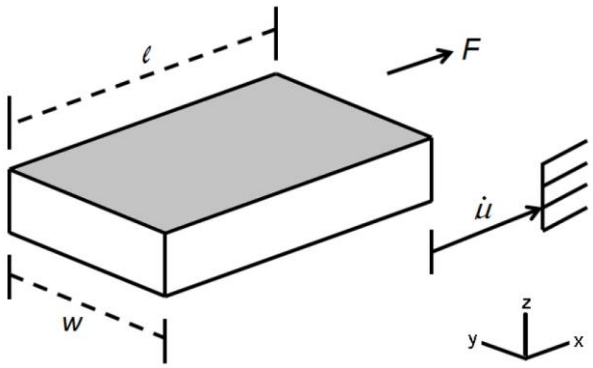


Figure 2.5 – Longitudinal mode rectangular plate resonator

For a rectangular plate resonator as shown in Figure 2.5, the lateral extensional (i.e., Length or Width Extensional Mode) vibration can be obtained from the analysis of a set of wave equations in [34], the wave equation in the x direction can be derived as:

$$\frac{E}{\rho}\frac{\partial^2 u}{\partial x^2} = -\omega^2 u \tag{2.7}$$

when only the force that generates stress in the $u(x)$ direction is considered; where E is Young's, ρ is material density and u is the displacement.

A general solution to Equation (2.7) is expressed as:

$$u(x) = A\sin kx + B\cos kx \tag{2.8}$$

where x is the coordinate in the length direction, and k is the propagation constant.

By applying boundary condition x = 0 to Equation (2.8), the value of A can be found as:

$$\frac{\partial u}{\partial x}\int_{x=l}^{x=0} = Ak\cos kx - Bk\sin kx = 0 \tag{2.9}$$

$$Ak\cos kx - 0 = 0 \text{ or } A = 0 \tag{2.10}$$

$$u(x) = B\cos kx \tag{2.11}$$

By applying another boundary condition x = l to Equation (2.9), the result is given as:

$$\sin kl = 0 \ , \text{ for } \quad k_n l = n\pi, n = 1, 2, 3, \ldots.. \tag{2.11}$$

Therefore, by substituting equation (2.11) into (2.7), k can be expressed as:

$$k = \omega\sqrt{\frac{\rho}{E}} \tag{2.12}$$

By substitute the values of k_n from Equation (2.11) into Equation (2.12), the resultant resonance frequency of a rectangular plate vibrating along its length in the nth mode:

$$f_n = \frac{n}{2l}\sqrt{\frac{E}{\rho}} \tag{2.13}$$

This analysis method can be extended to different geometries and mode shapes. For a circular disk Contour Mode (i.e., fundamental Extensional Modes), a similar approach can be used to derive the resonance frequency. The equation is given as:

$$f_{n\,(disk)} = \frac{a_n}{R}\sqrt{\frac{E}{\rho}} \tag{2.14}$$

where R is the radius of the resonator disk and a_n is a mode dependent scaling. Because circular disks resonator can achieve non-axisymmetric resonant modes as shown in the Figure 2.6, a proper approximation to a_n is needed. By assuming a Poisson's ratio μ = 0.3, the frequency scaling factor a_n for the first four disk fundamental Contour Modes selected with the aid of COMSOL Multiphysics® modal simulation are: a_1 = 0.272, a_2 = 0.342, a_3 = 0.418, and a_4 = 0.493 [35]. a_1

and a_2 are also known as the fundamental Wine Glass mode and the first Radial Contour mode, respectively.

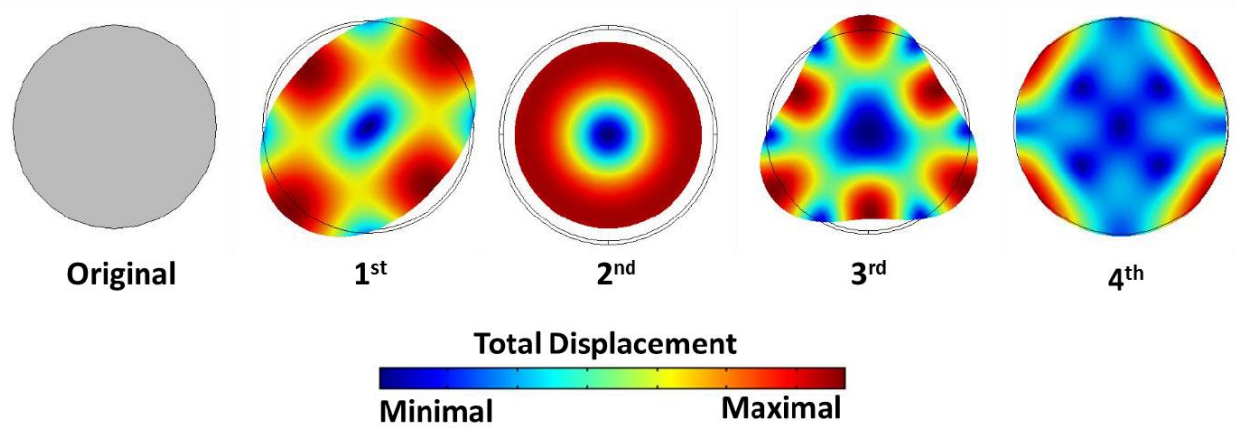


Figure 2.6 – FEM nodal analysis using COMSOL Multiphysics® of a circular membrane vibrating in the first 4 contour modes [10]

All the analysis of the resonator so far in this section is based on an ideal situation. The mechanical vibrating resonator body only consists the mass of piezoelectric material. However, a piezoelectrically-transduced resonator can't function as a proper electrical device without proper electrode layers or other structural layers. Thus, it is unavoidable to add the extra mass of those stacks to the vibrating body. Consequently, the attached mass attenuates and dissipates the energy in the system and causes the degradation of overall performance. This is so-called mass loading effect.

In order to include the mass loading effect to the prior discussed model, the equivalent acoustic velocity is introduced as:

$$v_{eq} = \sqrt{\frac{E_1T_1 + E_2T_2 + \cdots E_nT_n}{(\rho_1T_1 + \rho_2T_2 + \cdots \rho_nT_n)(1-\sigma^2)}} \tag{2.13}$$

where E, T, σ and ρ are the Young's modulus, thickness, Poisson's ratio, and density of each composite layers of a TPoS resonator, respectively. By substituting the equivalent acoustic velocity into

Equation (2.13), the modified resonance frequency of a TPoS in rectangular and disk shapes are expressed as:

$$f_n = \frac{n}{2l} v_{eq} \tag{2.14}$$

$$f_{n\,(disk)} = \frac{a_n}{R} v_{eq} \tag{2.15}$$

2.5 Electrical Circuit Representation of a MEMS Resonator

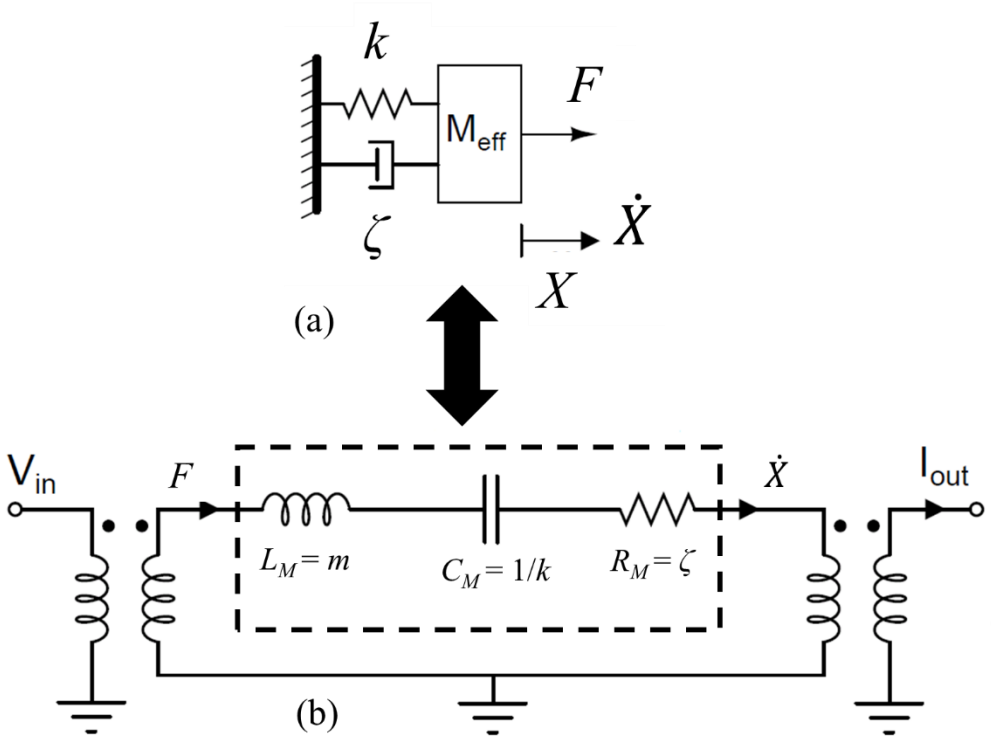


Figure 2.7 – (a) The lumped spring-mass model of a mechanical resonator; (b) the equivalent electrical model of an electromechanical resonator

For a typical MEMS resonator, the applied input electrical signal is first converted into force and then the force drive the resonator body into vibration. At the same time, the vibration of the piezoelectric material is converted back into an electrical signal at the output. In Figure 2.7 (a), the mechanical behavior of the resonator that depends on its physical properties can be represented

by a lumped element spring-mass-damper model. On the other hand, an equivalent electrical circuit model illustrated in Figure 2.7 (b) can also be built based on the mechanical-electrical analogy. An inductor, capacitor, and resistor in the electrical domain correspond to the inertia, compliance and damping in a mechanical system, respectively. The transductions from the electrical to the mechanical domain and vice versa can be modeled as transformers. The transduction factor (i.e., electromechanical coupling coefficients) can be defined according to transduction mechanism. Table 2.2 summarizes the analogy between the mechanical and electrical domain. In Figure 2.7 (b), an electrical voltage (U) at the input terminal is converted to a force (F) through a transduction factor η_{in} and a velocity ($\dot{X}$) at other output terminal is transduced to a current (I) through a transduction factor η_{out}.

$$F(t) = \eta_{in} U(t) \tag{2.16}$$

$$I(t) = \eta_{out} \dot{X}(t) \tag{2.17}$$

By assuming a harmonic motion at angular frequency $\omega_0 = 2\pi f_0$, and neglecting any phase information, Equation (2.16) and Equation (2.17) can be written as:

$$F = \eta_{in} U \tag{2.18}$$

$$I = \eta_{out} \omega_0 X \tag{2.19}$$

where X donates the displacement. At resonance frequency, the imaginary part of the impedance is canceled and real part of the impedance is purely resistive. Thus, the motional resistance R_M of the resonator is given as:

$$R_M = \frac{U}{I} = \frac{F}{\eta_{in}\eta_{out}\omega_0 X} \tag{2.20}$$

Relating the motional resistance with the mechanical parameters and the transduction factor, Equation (2.20) can be given as:

$$R_M = \frac{\zeta}{\eta_{in}\eta_{out}} \tag{2.21}$$

The reactive components L_M and C_M can be also obtained:

$$L_M = \frac{m}{\eta_{in}\eta_{out}} \tag{2.22}$$

$$C_M = \frac{k}{\eta_{in}\eta_{out}} \tag{2.23}$$

Table 2.2 – Analogy between electrical and mechanical domain

Mechanical Domain	**Electrical Domain**
Force, F	Voltage, V
Velocity, $\dot{X}$	Current, I
Displacement, X	Charge, q
Mass, m	Inductance, L_M
Compliance, $1/k$	Capacitance, C_M
Damping, ζ	Resistance, R_M

2.6 Butterworth-Van Dyke (BVD) Circuit Model

The most classic lumped-element Butterworth-Van Dyke (BVD) circuit model is initially used to model the operation around the resonance of a quartz crystal resonator. The model is not only very useful to describe the electrical behavior of an electrically-transduced mechanical resonator, but also applicable for piezoelectrically-transduced and capacitive-transduced resonators. Nowadays, the BVD model is widely used for AlN Thin-Film Bulk Acoustic Resonators (FBARs) and Surface Acoustic Wave (SAW) resonators.

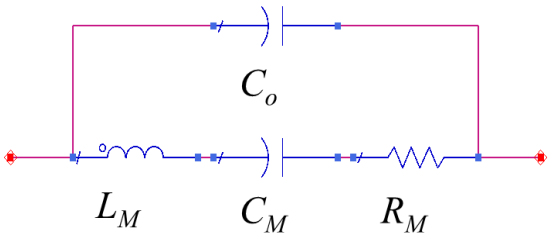


Figure 2.8 – Butterworth-Van Dyke (BVD) circuit model

In the BVD circuit model shown in Figure 2.8, the transduction mechanism of the resonator is represented by the motional inductance L_M, motional capacitance C_M and motional resistance R_M in series, which corresponding to the mass, compliance, and dimpling in the mechanical domain of the resonator. C_O in the other parallel branch describes the shunt capacitance between the electrodes. The impedance (Z) and unloaded quality factor (Q_U) of the BVD circuit are given as:

$$Z(s) = \frac{s^2 + \left(\frac{R_M}{L_M}\right)s + {\omega_s}^2}{1 + sR_M C_o + \frac{C_O}{C_M} + s^2 L_M C_o} \tag{2.24}$$

$$Q_U = \frac{\omega_s L_M}{R_M} = \frac{1}{\omega_s C_M R_M} \tag{2.25}$$

where ω_s is the series resonance frequency:

$$\omega_s = 2\pi f_s = \frac{1}{\sqrt{L_M C_M}} \tag{2.26}$$

and the parallel resonance (i.e., the anti-resonance) frequency can be written as:

$$\omega_a = 2\pi f_a = \omega_s \left(1 + \frac{C_M}{C_o}\right)^{1/2} = \frac{1}{\sqrt{L_M \frac{C_M C_o}{C_{M+} C_o}}} \tag{2.27}$$

The square of the electromechanically coupling coefficient (k_{eff}) is the most important parameter used among the specifications of the piezoelectrically-transduced resonator. It is generally defined as the ratio of electrical (mechanical) energy stored in the volume of a

piezoelectric body and the capability of conversion to the total mechanical (electrical) energy supplied to the body [36]. Thus, combining with the quality factor (Q), the figures of merit (FoM) of a resonator is given by the product of Q and k_{eff}^2.

Using the mechanical energy (U_M) and electrical energy (U_E) of the resonator body, k_{eff}^2 can be expressed [37] as:

$$k_{eff}{}^2 = \frac{U_M}{U_E + U_M} = \frac{\frac{1}{2}C_M V^2}{\frac{1}{2}C_o V^2 + \frac{1}{2}C_M V^2} = \frac{C_M}{C_o + C_M} \approx \frac{C_M}{C_o} \tag{2.28}$$

To experimentally determine k_{eff}^2 by measuring the series resonance and anti-resonance frequencies, k_{eff}^2 can be further extended as [36]:

$$k_{eff}{}^2 == \frac{\omega_a{}^2 - \omega_s{}^2}{\omega_a{}^2} \tag{2.29}$$

Specifically, for FBAR vibrating in the thickness-mode (i.e., Mode 33), the longitudinal coupling coefficients (k_{33}^2) which measures the electromechanical conversion efficiency in the c-axis ("3") when an electric field in the z-axis ("3") is applied to the piezoelectric, is defined from the experimental results as [38][39]:

$$k_{33}{}^2 = \frac{\pi^2}{4}\frac{\omega_s}{\omega_a}\frac{\omega_a - \omega_s}{\omega_a} = \frac{\pi^2}{4}\frac{f_s}{f_a}\tan\left(\frac{\pi}{4}\frac{f_a - f_s}{f_a}\right) \tag{2.30}$$

CHAPTER 3: DEVELOPMENT OF ZNO THIN-FILM PIEZOELECTRICALLY-TRANSDUCED RESONATOR

In this chapter, the development of ZnO thin-film piezoelectric-on-substrate (TPoS) resonators is thoroughly discussed. Firstly, fabrication processes of resonators built on Silicon-on-Insulator (SOI) wafer and Diamond-on-Silicon (DOS) wafer are presented and illustrated in details. Depends on the materials and stack configuration of the substrate used, the fabrication process can be completely different. When the resonator is fabricated on SOI, pre-release process is preferred whereas the resonator on Diamond is fully suspended at the last step of the fabrication process. Secondly, FEM simulation of ZnO TPos resonators is carried out to enhance the understanding of the resonance modes and to promote the resonator design in the future. Thirdly, the frequency response of fabricated devices is rigorously measured and compared with simulation results, along with temperature dependence of the resonator on different substrates. Lastly, complete circuit models including classic Butterworth-Van Dyke (BVD) circuit model and substrate model are explained and demonstrated.

3.1 Fabrication Process of ZnO Piezoelectric Resonator on Silicon-on-Insulator Wafer

The piezoelectric resonators are fabricated using a silicon-on-insulator (SOI) wafer and a five mask photo-lithography process. A 2 μm thick SiO_2 insulator layer and a 10 μm thick silicon structural layer are used, which are due to the compromise of motional resistance and quality factor of the resonator from prior experimental results and conclusions. As silicon device layer getting thinner, the ZnO piezoelectric layer becomes a larger portion of the resonator body. Therefore, the electromechanical coupling coefficient is enhanced. However, at the same time, a slight

degradation in the quality factor is expected due to a larger acoustic loss in ZnO layer as compared to that of single crystal silicon.

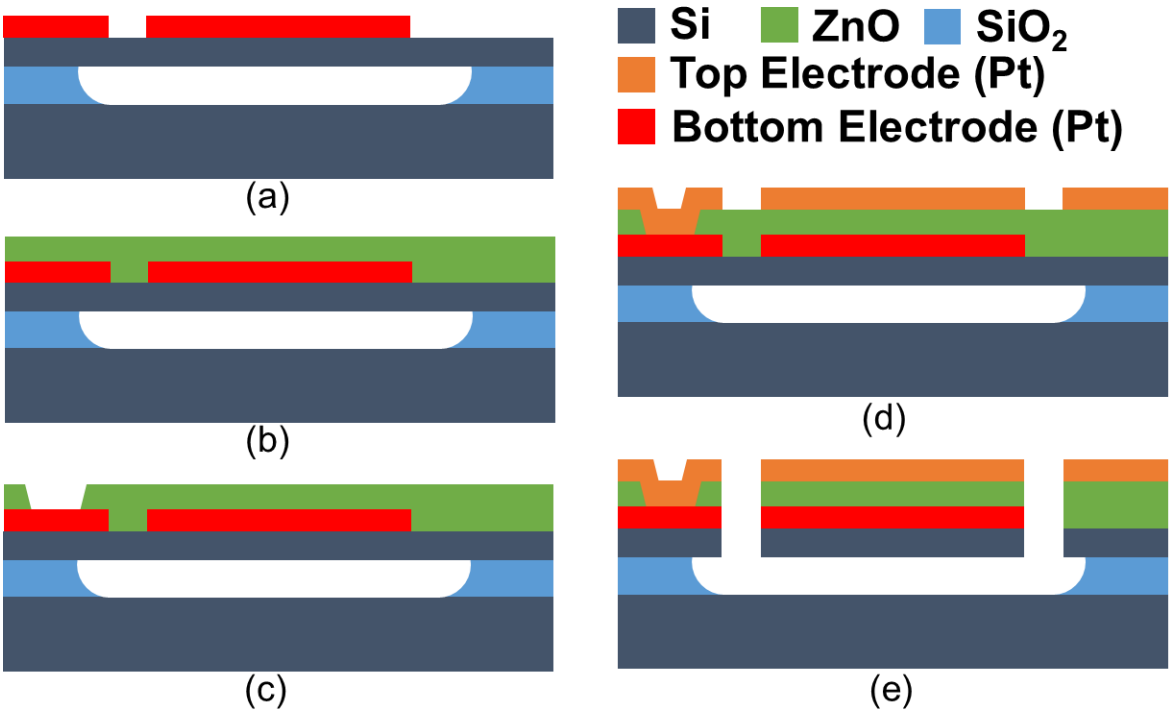


Figure 3.1 – Five-masks Fabrication Process of ZnO Piezoelectric Resonator on Silicon-on-Insulator Wafer: (a) resonator pre-release and bottom electrode (Cr+Pt) patterning by lift-off; (b) sputtering deposition of the piezoelectric ZnO film; (c) etch vias through ZnO for the bottom electrodes access; (d) deposition and patterning of top electrodes; (e) ZnO dry etch followed by Silicon dry etch

As the first step, the pre-release process is done by first etching a series of release holes around the resonator body in the silicon device layer followed by wet isotropic etching to remove the buried oxide layer underneath using 49% hydrofluoric acid (HF) solution. The bottom electrodes are formed by sputtering 30 nm Chrome (Cr) as an adhesion layer and 170 nm Platinum (Pt) as the main conductor. Then, bottom electrodes are patterned by lift-off and followed by the sputtering deposition of 500 nm ZnO piezoelectric layer. The optimized process condition for ZnO RF sputtering deposition is 300 ˚C for substrate temperature, 5 mTorr for plasma pressure, 1:1 Ar: O2 ratio with a total of 12 sccm gas flow, and 100 W for RF power. Subsequently, openings to

contact the bottom electrodes are wet etched through ZnO in a mixed solution of 1: 200 HCl: H_2O. 200 nm top electrodes are then deposited using the same process for bottom electrodes. ZnO is dry etched with CH_4-Ar plasma by reactive ion etching. Finally, the device resonator body is defined and released by a silicon anisotropic deep reactive ion etching (DRIE) process to cut through the pre-released device layer already suspended over the SOI substrate. Fig. 3.1 (a) – (e) illustrate the cross-sectional process flow of the major fabrication steps.

3.2 Fabrication Process of ZnO Piezoelectric Resonator on Diamond-on-Silicon Wafer

Figure 3.2 presents the fabrication process flow of the piezoelectric resonators which are built on Diamond-on-Silicon substrate. Unlike using SOI as the substrate and pre-release of the device layer is not required, this process not only simplifies the fabrication steps by reducing one photomask but also removes the risk of collapsing the resonator body during the fabrication process due to the striction issue. This process starts with bottom electrodes deposition using sputtering that are patterned by lift-off. Then, ZnO, as a piezoelectric layer, uniformly covers the entire wafer by a RF sputtering deposition. The top electrodes deposition and via filling are done at the same time once vias are opened to the bottom electrodes by diluted hydrochloric acid wet etch. In order to etch through Diamond layer and eventually undercut the silicon underneath to suspend the resonator, an effective hard mask is critically needed for the dry releasing process. 2 µm PECVD SiO_2 is used to serve the purpose because it has a very high selectivity of 1:15 against the diamond dry etching recipe using pure O_2 plasma while also offering extremely high selectivity of 1:3000 against silicon isotopic etch using SF_6. Once the SiO_2 hard mask is patterned using standard lithography process and a RIE process, ZnO layer is first etched with CH_4-Ar plasma and then the diamond layer can be etched with very high RF power of 2800 W with additional 300 W substrate biasing power in an O_2 plasma. Substrate biasing power needs to be as high as possible

to ensure a vertical etch profile. At last, the silicon underneath the resonator body area is etched through undercut by using a SF_6-based dry release process.

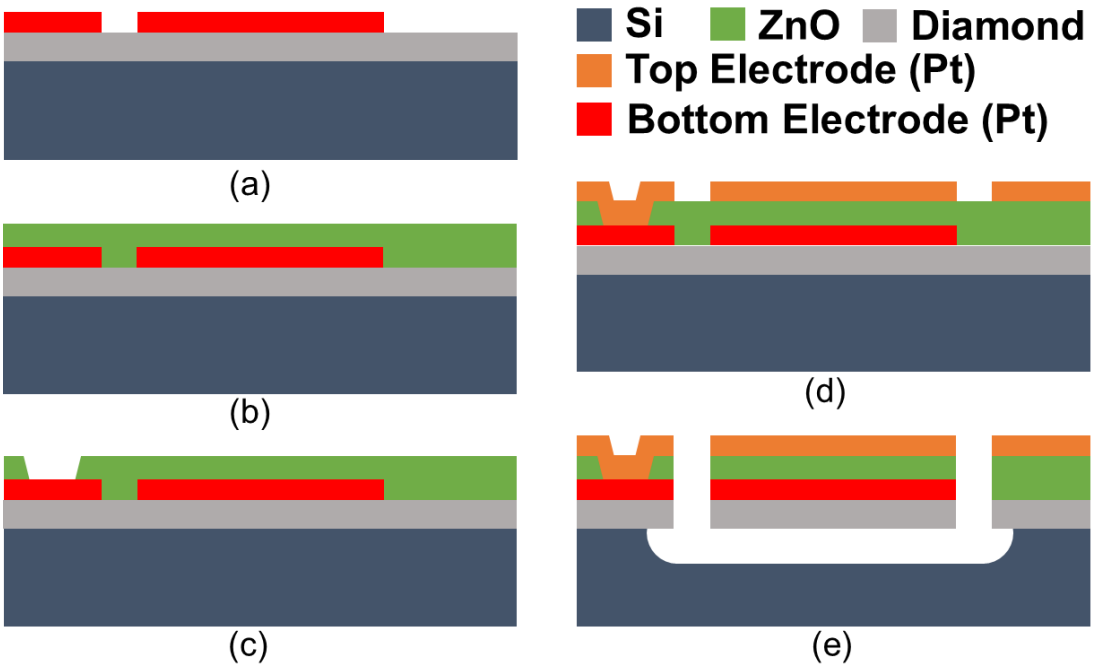


Figure 3.2 – Four-masks Fabrication Process of ZnO Piezoelectric Resonator on Diamond-on-Silicon Wafer: (a) bottom electrode (Cr+Pt) deposition and patterning by lift-off; (b) sputtering deposition of the piezoelectric ZnO film; (c) etch vias through ZnO for bottom electrodes access; (d) deposition and patterning of top electrodes; (e) ZnO dry etch followed by Diamond dry etch and Silicon isotropic dry release

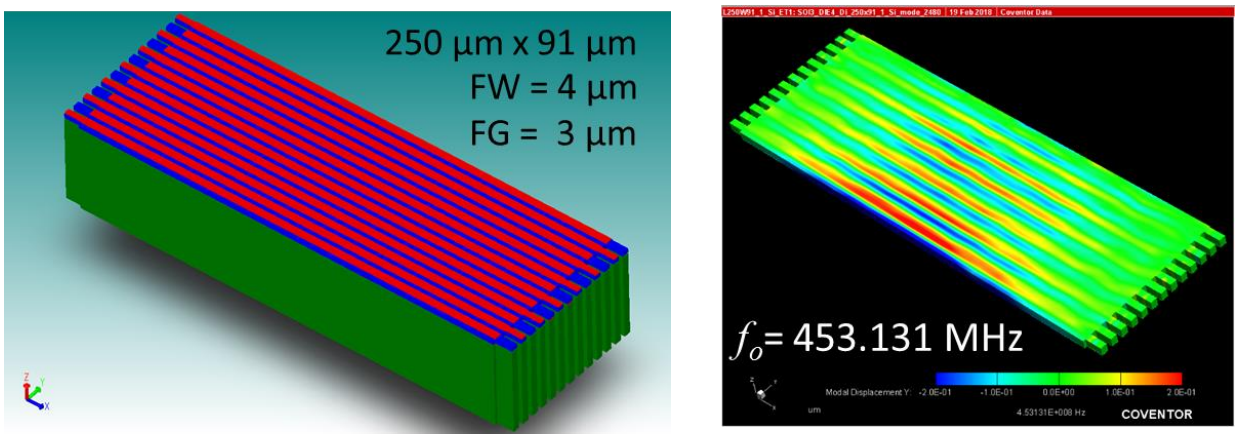
3.3 Simulation of ZnO Thin-film Piezoelectric-on-Substrate (TPoS) Resonator

In order to visualize the resonance modes of the piezoelectric resonator in a 3-D view and predict the performance of designed resonator in the frequency domain, a study of a finite element method (FEM) simulation is carried out in this section. MemMech is a mechanical solver in CoventorWare that is a popularly used FEM simulator. The piezoelectric analysis in MemMech is chosen to simulate the frequency response of thin-film piezoelectrically-transduced resonators, as well as any other devices that use piezo effects because the solver for piezoelectric analysis can compute the internal strain and internal electrical response resulted from an externally imposed electric field or charge distribution. Since potential boundary condition has been applied to at least

one surface in each dielectric region, the structural layers of the resonator such as silicon, siO_2, and diamond are manually set to be conductors. It is recommended to specify a very large number e.g., 5,000) for the number of modes in the simulation setup due to the fact that the simulation capture all of the modes including countless spurious modes (many with very weak amplitudes) in the specified frequency range. It's required to set up the surface BC potential as 0V as well as harmonic surface BC potential as 1V in modal harmonic simulation within the piezoelectric analysis. Material properties such as Young's modulus, Poisson's ratio, and density used in the resonator structure are summarized in Table 3.1.

Table 3.1 – Material properties for the resonator body

	E (MPa)	Poisson	Density(kg/um^3)
Diamond	1.22E+06	2.00E-01	2.35E-15
Silicon	1.30E+05	2.78E-01	2.33E-15
Platinum	1.45E+05	3.50E-01	2.14E-14



(a) (b)

Figure 3.3 – (a) 3-D view of a ZnO thin-film piezoelectric rectangular resonator on SOI with a body dimension of 250 µm x 91 µm, finger number of 13, finger pitch size of 7 µm, finger width of 4 µm and 13 tethers; (b) Modal displacement in Y direction of the 13th order width-extensional (WE) mode

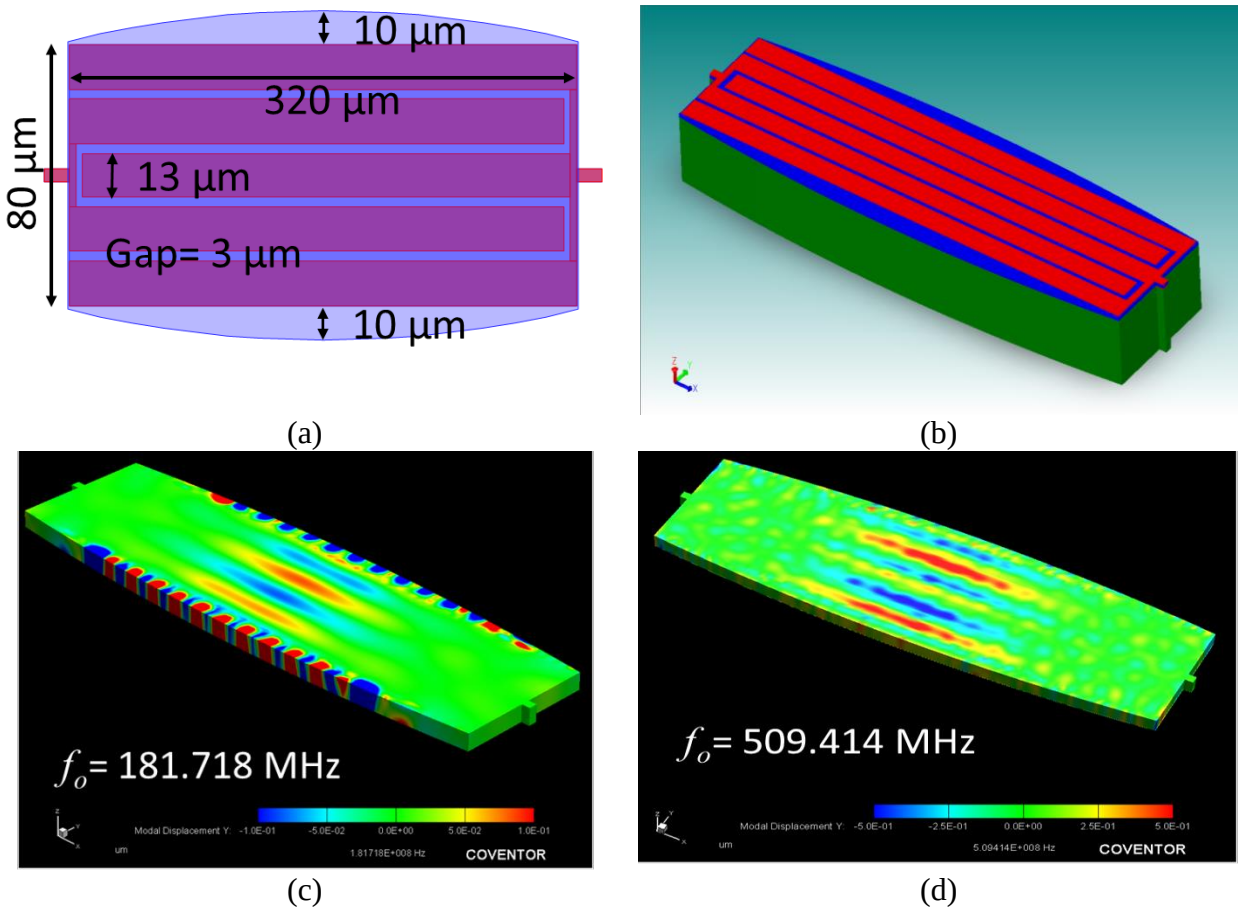


Figure 3.4 – (a) A ZnO thin-film piezoelectric rectangular resonator on Diamond-on-Si with 10 µm wide curvature body that has a body dimension of 320 µm x 80 µm, finger number of 5, finger pitch size of 16 µm, finger width of 13 µm and 1 pair of tethers; (b) 3-D view of the resonator in CoventorWare; (c) modal displacement in Y direction of the 2nd order width-extensional (WE) mode; (d) modal displacement in Y direction of the 3rd order WE mode

A conventional design of a two-port ZnO thin-film piezoelectric rectangular resonator on ZnO-on-Si is proposed for CoventorWare simulation study. Using the fabrication process developed in the previous section, a 3-D model of the resonator is successfully generated in Figure 3.3 (a). Four stacked layers from top to bottom are top electrodes in red, ZnO in blue, bottom electrode in red and Silicon device layer in green. Thirteen interdigital fingers with a finger width of 4 µm and finger gap of 3 µm are situated on top of the 250 µm x 91 µm rectangular ZnO plate. The model simulation in piezoelectric analysis successfully demonstrates that the 13th order width-

extensional (WE) has a resonance frequency of 453.131 MHz. The profile of modal displacement in the Y (lateral width) direction is shown in Figure 3.3 (b).

Figure 3.4 (a) depicts the layout of a rectangular resonator with 10 µm wide curved resonator body on each side. This resonator is designed to be 320 µm x 80 µm in dimension with a finger width of 13 µm and finger gap of 3 µm. The effect of curved resonator body is experimentally demonstrated by changing the curvature width up to the acoustic wavelength (λ) of the Lamb wave to provide a consistent increase in quality factor [40]. The 3-D structure of the resonator for simulation is shown in Figure 3.4 (b). The modal displacement in the Y (lateral width) direction of the 2^{nd} and 3^{rd} order width-extensional (WE) analysis from simulation results are shown in Figure 3.4 (c) and (d) respectively.

It's very helpful to use FEM simulation by CoventorWare to find the vibrational modes and the corresponding resonance frequencies. However, co-solver is needed to predict the quality factor at the resonance since the loss mechanism can't be included in a standalone piezoelectric analysis. In addition, the frequency responses of the resonators in S-parameter are intensively simulated by using FastPZE. The simulated results are plotted along with the measurement data for comparison in the following section.

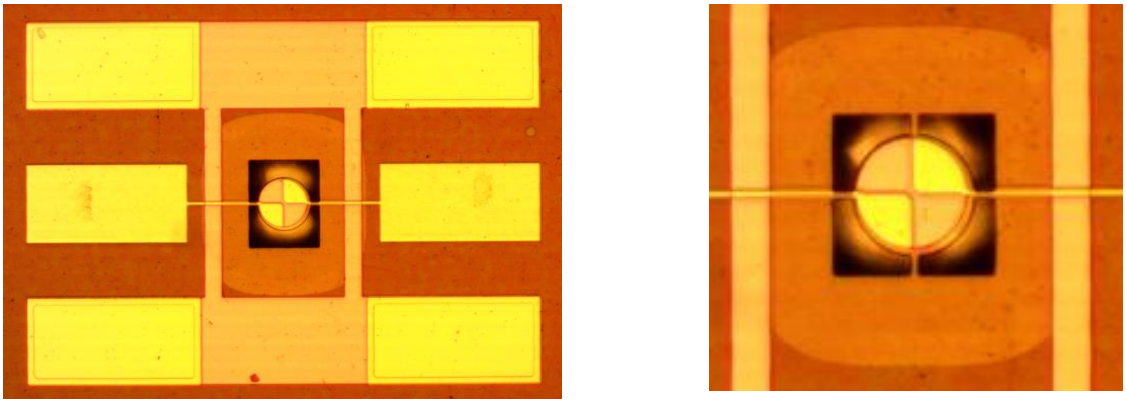
3.4 Experimental Results of ZnO TPoS Resonator

3.4.1 Contour Modes in TPoS Resonators

The micro-fabricated ZnO Piezoelectrically-Transduced resonators are tested on a Cascade RF probe station in the air under atmospheric pressure and room temperature. The scattering parameters (S-parameters) of these two-port resonators are measured directly with the on-wafer probing method using an Agilent 8753ES vector network analyzer. A Short-Open-Load-Thru

(SOLT) calibration is performed on a CS-5 calibration substrate (GGB Industries Inc.) to de-embed the loss from RF cables and probes.

Thin-film ZnO piezoelectric disk resonators with a radius of 30 μm and tether length of 10.5 μm are measured in their radial contour and wineglass modes. Both two-tether design and four-tether of the disk resonators are fabricated with dimensions except tether number on Diamond-on-Silicon wafer. They are tested in a two-port configuration. Figure 3.5 (a) shows a fabricated two-tether disk resonator including the probe pads on each side for the two-port measurement. Zoom-in view of a four-tether design in Figure 3.5 (b) clearly shows additional two tethers located in upper and lower sides of the disk resonator body. The frequency response plotted in Figure 3.6 presents resonance frequency of fundamental Wine Glass mode at 213.47 MHz and Contour Mode at 190.38 MHz for two-tether 30 μm-radius disk resonator. Because of the additional two tethers are located at the quasi-nodal points, it is observed that the Wine Glass Mode and some higher order of Contour Mode are knocked out for four-tether disk resonator as expected.



(a) (b)

Figure 3.5 – (a) Actual photograph of a two-port two-tether 30 μm radius disk resonator fabricated on a SOI wafer with 10 μm thick silicon device layer; (b) zoom-in view of a 30 μm radius disk resonator with the four-tether design

Another disk resonator is fabricated with a radius of 40 μm on Diamond-on-Silicon and its fundamental Contour Mode is captured within a narrow frequency range of 10 MHz. As a result,

the resolution is high enough to calculate the loaded quality factor of the resonance using -3 dB bandwidth method as shown in Figure 3.7. The disk resonator exhibits a loaded quality factor of 4,678.1 with resonance peak insertion loss of -38.11 dB in its fundamental Radial-Contour mode.

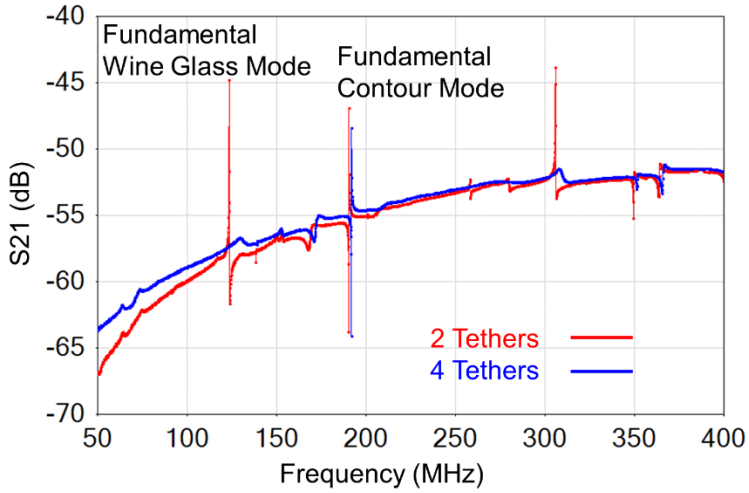


Figure 3.6 – Measured frequency response (S_{21} in dB) of the 30 µm radius disk resonators fabricated on a SOI wafer: 2-Tether Design vs. 4-Tether Design

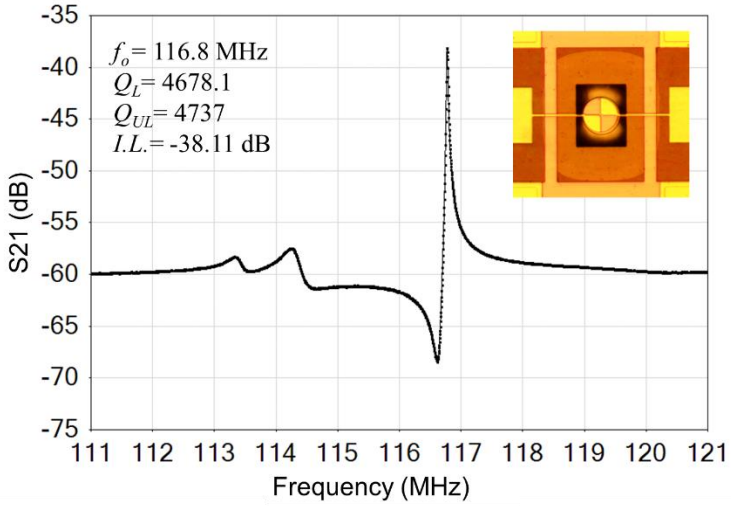


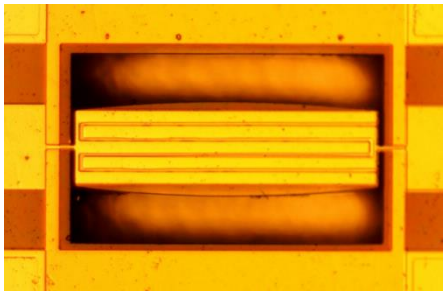
Figure 3.7 – Measure frequency response (S_{21} in dB) of a 40 µm radius disk resonator on SOI in fundamental Radial-Contour mode

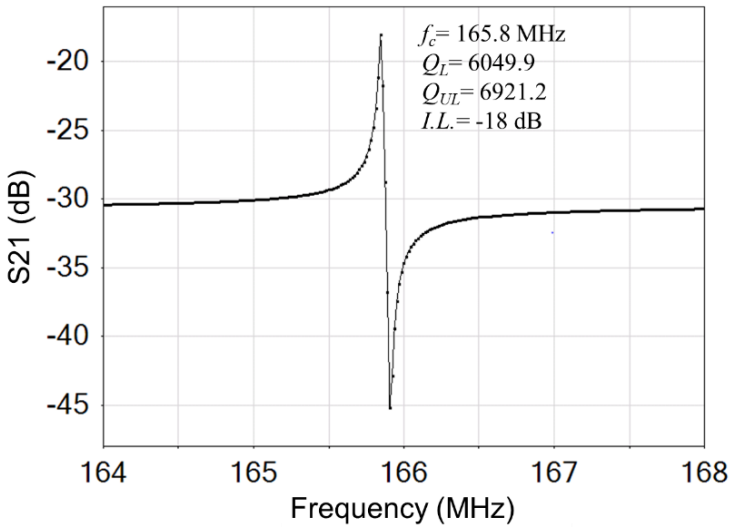
A 320 µm x 80 µm rectangular resonator with 10 µm wide curved resonator body is fabricated on Diamond-on-Silicon substrate and it is demonstrated in Figure 3.8 (a). The tether

length and width are designed to be the minimal feature size (i.e., 5 μm) that USF fabrication facility can offer repeatedly because smaller tether size is experimentally proven to have a lower acoustic energy loss in general. Figure 3.8 (b) presents in the 2nd order width-extensional mode. The resonance has a center frequency of 165.8 MHz with a loaded Q of 6,049.9 in the air. Unloaded Q is calculated to be 6921.2 from Equation (4.6). Usually, the piezoelectric MEMS resonator can achieve a *Q* in a range of 500 to 3,000 largely due to the high energy dissipation (low-*Q*) of piezoelectric transducer layer that is typically caused by the non-uniform stress distribution between multiple material stacks [41-43]. The insertion loss of the resonance peak is 18 dB and the associated motional resistance including the top electrode conductive loss is therefore calculated to be 694.3 Ω. Despite this resonator has a decent high quality factor, the insertion loss is still too high for filter applications at least with standard 50Ω termination impedance. Since the interdigitated finger width (i.e., 13 μm) is designed to be much wider than the gaps between metal fingers (i.e., 3 μm), it is expected to have much higher static capacitance between top electrodes. However, it is a bit disappointing that the wider electrode doesn't collect more charges. Consequently, the feedthrough level of the resonator is -30 dB and the power level difference between the resonance peak and feedthrough level is only 12 dB.

Based on the prior resonator design with curvature body and regular tethers, a modified tether design is implemented and presented in Figure 3.9 (a). A so-called Phononic Crystal (PC) strip tether is designed that is composed of 6 periodical cross-shaped slabs with equal length of 5 μm for all the sides. Recently, PC design for high *Q* piezoelectric MEMS resonator has attracted great attention because it is well known that PC structures can generate acoustic band gaps where the mechanical vibration and acoustic wave propagation are not allowed [44]. Furthermore, PC tethers can reduce the energy loss from the resonator body through the anchors by eliminating

vibration and preventing acoustic wave propagation through the attached tethers [44]-[48]. The PC cross shape tether design is first introduced in [49] to reduce the tether loss as well as to significantly increase the *Q* of AlN Lamb wave resonators.

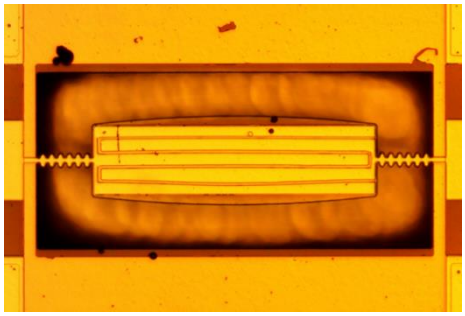


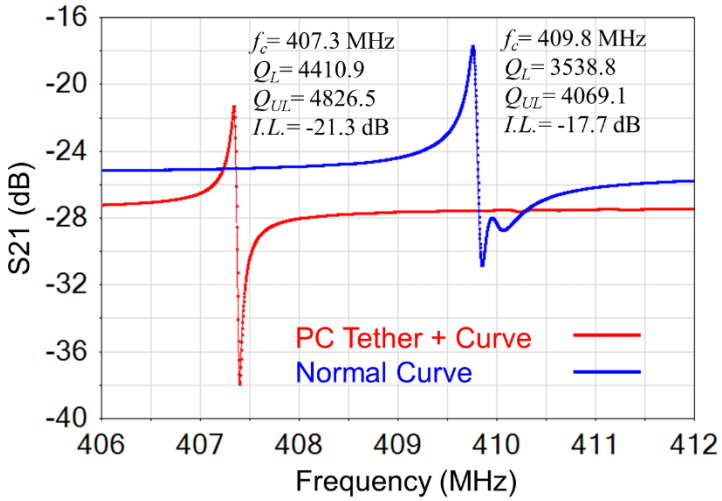


(a) (b)

Figure 3.8 – (a) Actual photograph of a ZnO thin-film piezoelectric rectangular resonator with curvature body on Diamond-on-Si that has a body dimension of 320 µm x 80 µm, finger number of 5, finger pitch size of 16 µm, finger width of 13 µm and 1 pair of tethers; (b) measured frequency response (S_{21} in dB) of the resonator

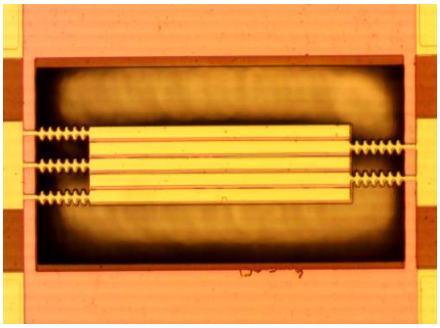
For direct comparison, the frequency response of the measured resonance around 408 MHz for both regular tether and Phononic Crystal (PC) tether devices are plotted in Figure 3.9 (b). The resonator using PC tethers has shown a loaded *Q* of 4,410.9, which reveals a 24.6% *Q* improvement as compared to the design with regular tethers even though the total length for the PC tether is 13 times longer. It is obvious that PC tether doesn't significantly change the resonance frequency or introduce any spurious modes while offering a significant improvement to quality factor. Therefore, the PC structures can serve as the acoustic energy insulators for the designed frequencies.

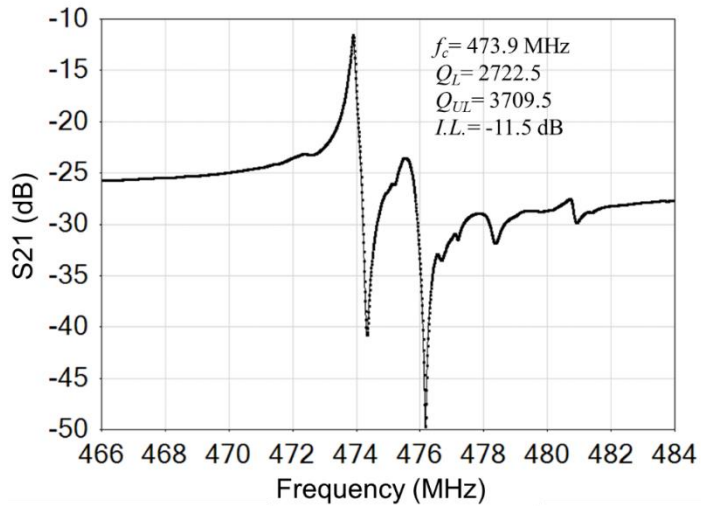




(a) (b)

Figure 3.9 – (a) Actual photograph of a ZnO thin-film piezoelectric rectangular resonator with curvature body on Diamond-on-Si that has 1 pair of Phononic Crystal (PC) strip tethers; (b) measured frequency response (S_{21} in dB) of the resonators with PC tether design and normal tether design





(a) (b)

Figure 3.10 – (a) Actual photograph of a ZnO thin-film piezoelectric rectangular resonator on Diamond-on-Si that has 5 Phononic Crystal (PC) strip tethers; (b) measured frequency response (S_{21} in dB) of the resonator

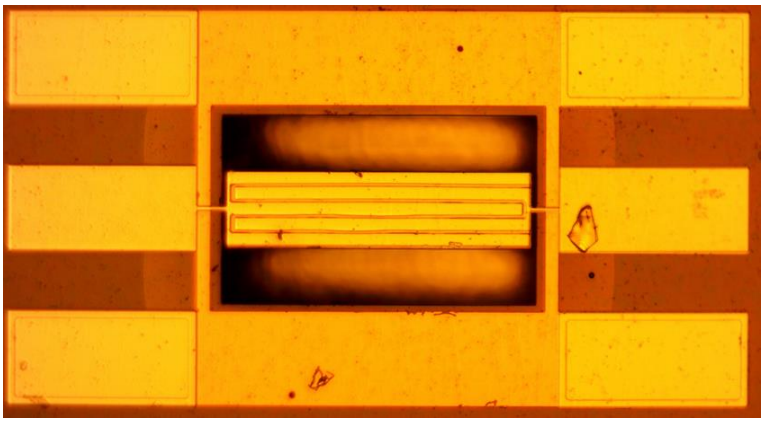
Figure 3.10 presents a 320 µm x 80 µm resonator with the multiple-tether design. Usually, multiple tethers are needed not only for effectively eliminating spurious modes but also for higher

power handling capability. Due to the reason that more tethers introduce more anchor loss, all the tethers are reasonably replaced by Phononic Crystal (PC) tether design to prevent acoustic energy loss. The resonance centered at 473.9 MHz shows its loaded *Q* of 2,722.5 and insertion loss of 11.5 dB as seen in Figure 3.10 (b). The calculated unloaded *Q* reaches 3,709.5 and the motional resistance of the resonator is 275.8 Ω, which makes it a qualified candidate as a tank circuit for an oscillator design.

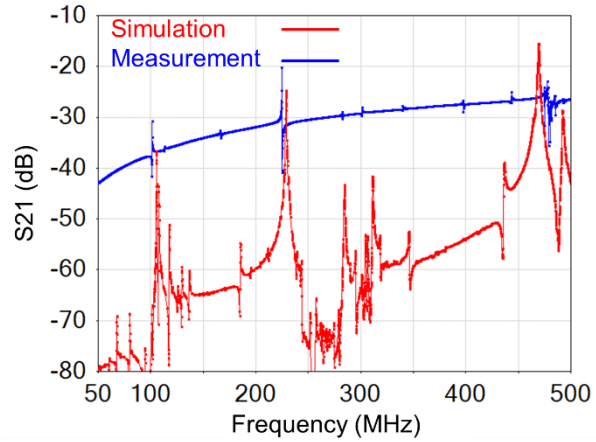
3.4.2 Comparison of Measurement and Simulation Results

To facilitate future design of ZnO piezoelectric resonators, it is critical to match the simulation prediction with actual measurement results of the fabricated devices. More importantly, the actual material parameters can be refined during the fitting process.

Figure 3.11 (a) shows a basic rectangular plate ZnO piezoelectric resonator on Diamond-on-Silicon. Its frequency response in S_{21} and Y_{11} are plotted in Figure 3.11 (b) and (c). Despite the fact that the feedthrough level of the simulation and measurement are different because the parasitic effects of probing pads and substrate loss are not taken into account, the resonance frequencies for all 3 major vibrational modes at 102.37 MHz, 234.02 MHz, and 479.97 MHz are all matched very well. The frequency discrepancies for each corresponding resonance mode is within 3%. The composited acoustic velocity of the resonator with the ZnO-on- diamond stacked resonator structural layer is calculated to be 15,359 m/s from the product of the frequency and wavelength. Thus, having a diamond as a device structural layer has led to increase of the acoustic velocity of the resonator operating in Contour Mode, which is about twice as compared to that of a silicon counterpart. Meanwhile, such strong agreement between simulation and measurement also validate that the simulation boundary conditions and material parameters are given correctly.



(a)



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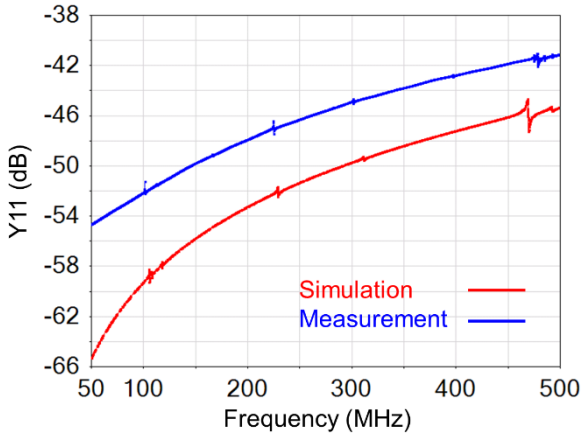
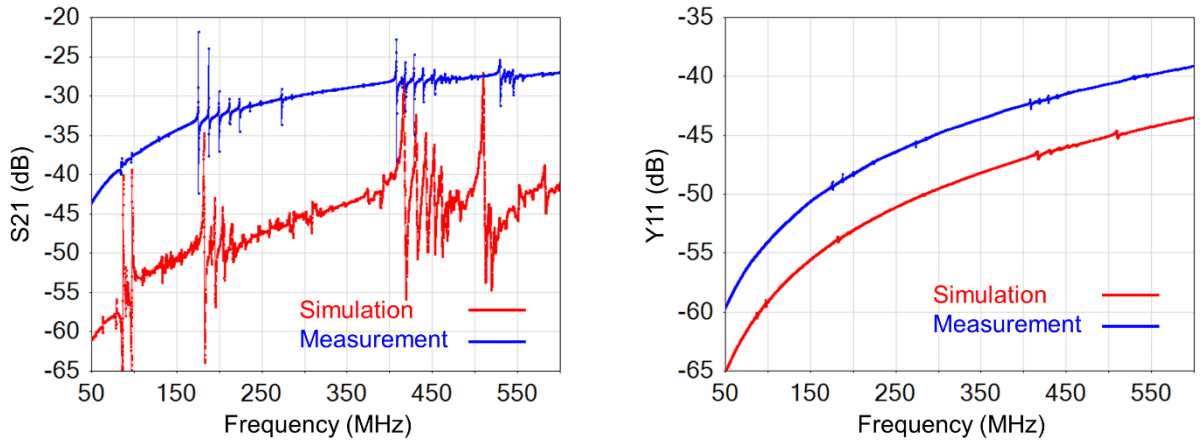


(c)

Figure 3.11 – (a) Actual photograph of a ZnO thin-film piezoelectric rectangular resonator on Diamond-on-Si that has a body dimension of 320 µm x 80 µm, finger number of 5, finger pitch size of 16 µm, finger width of 13 µm and 1 pair of tethers; (b) measured and simulated frequency response (S_{21} in dB) of the resonator; (c) measured and simulated frequency response (Y_{11} in dB) of the resonator

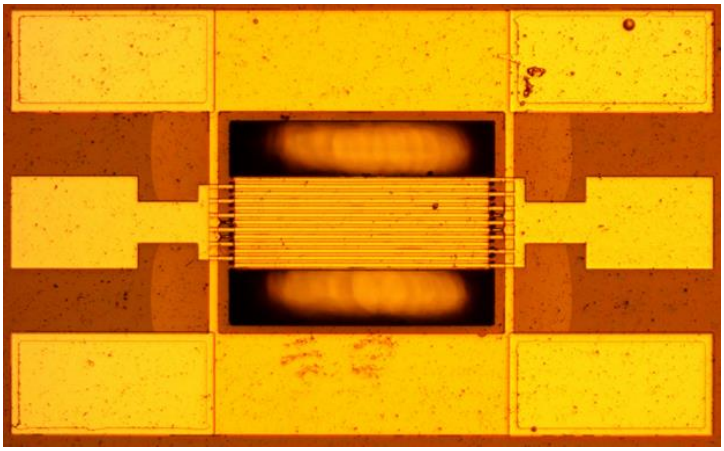
The resonator with a curved body shape as shown in Figure 3.8 (a) is also simulated and its S-parameter results are plotted in Figure 3.12 (a) and (b). Comparing the simulated result in red to the measured data in blue, it is worthy to note that every major resonance modes, especially numbers of spurious modes are precisely captured by simulation in CoventorWare. The frequency discrepancy for each corresponding resonance is less than 4%.



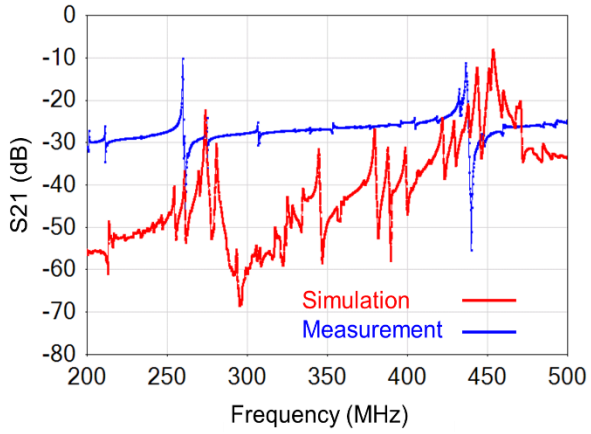
(b) (c)

Figure 3.12 – (a) measured and simulated frequency response (S_{21} in dB) of a 320 µm x 80 µm curvature resonator on Diamond-on-Si shown in Figure 3.8 (a); (b) measured and simulated frequency response (Y_{11} in dB) of the resonator

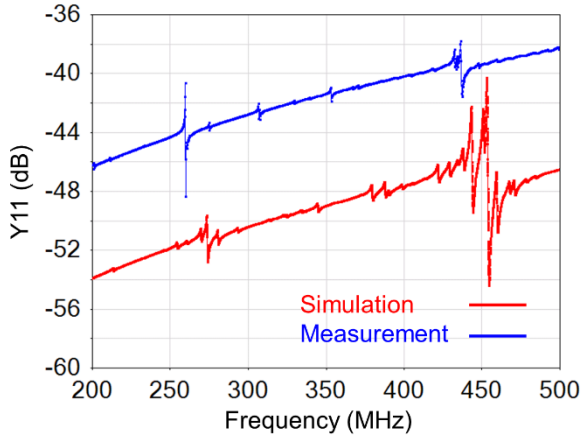
Figure 3.13 (a) presents a thirteen-tether resonator that has its resonator body of 251 µm x 91 µm on a SOI substrate with finger width of 4 µm and a finger width of 3 µm. Although two major resonance peaks are successfully matched with slightly larger tolerance in Figure 3.13 (b) and (c), a few spurious modes near major resonances are not eliminated by the tether boundary setup. These results suggest that CoventorWare simulation is insufficient or unable to remove the spurious mode by simply locking the tether nodal point in the simulation. From the simulation, the composited acoustic velocity of the stacked resonator structural layer including the silicon device layer is calculated to be 6,107.5 m/s which is lower than the acoustic velocity of ZnO due to the reason that all the electrodes are made of Platinum, whose acoustic velocity is merely 3,300 m/s.



(a)



(a)



(b)

Figure 3.13 – (a) Actual photograph of a ZnO thin-film piezoelectric rectangular resonator on SOI with a body dimension of 250 µm x 91µm, finger number of 13, finger pitch size of 7 µm, finger width of 4um and 13 tethers; (b) measured and simulated response (S_{21} in dB) the resonator; (c) measured and simulated response (Y_{11} in dB) the resonator

Table 3.2 summaries the comparison of measurement and FEM simulation results for various designs of ZnO TPoS resonators. Although the finite element method analysis can accurately predict the resonance frequencies with mode shapes accordingly for each resonator design, CoventorWare is not capable of correctly simulating the *Q* rather than leveraging an assigned damping ratio (total energy dissipation factor). It is more practical to measure the quality factor of the micro-fabricated resonator due to the process variations

Table 3.2 – Comparison of measurement and FEM simulation results for various designs of ZnO TPoS resonators

	Device Parameters							Simulation SOI 10μm	Simulation DOS 10μm	Measurement SOI 10μm	Measurement DOS 10μm	Simulation	Measurement		
Device Name	Length (μm)	Width (μm)	Finger Number	Finger Width (μm)	Finger Gap (μm)	Pitch Size (μm)	Number of Tethers (Pair)	Resonant Frequency (MHz)	Resonant Frequency (MHz)	Resonant Frequency (MHz)	Resonant Frequency (MHz)	DOS/SOI Frequency Ratio	DOS/SOI Frequency Ratio	SOI Discrepancy (%)	DOS Discrepancy (%)
L250W91	250	91	13	4	3	7	13	273.36	527.57	259.63	574.66	1.93	2.21	5%	-8%
								452.97	780.49	436.25	911.72	1.72	2.09	4%	-14%
L140W80	140	80	6	10.3	3	13.3	1	141.34	290.75	N/A	271.73	2.06	N/A	N/A	7%
								249.11	516.32	N/A	555.74	2.07	N/A	N/A	-7%
L200W90	200	90	9	7	3	10	9	191.96	395.23	162.21	383.73	2.06	2.37	18%	3%
								287.39	570.23	N/A	N/A	1.98	N/A	N/A	N/A
								347.54	620.41	340.64	694.96	1.79	2.04	2%	-11%
L320W80 #1	320	80	5	13	3	16	1	55.12	105.52	46.51	102.37	1.86	2.20	19%	3%
								109.39	228.95	83.01	234.02	2.14	2.82	32%	-2%
								218.72	469.27	227.18	479.97	2.19	2.11	-4%	-2%
L320W80 #2											101.63		2.19		
											226.83		2.73		
											478.13		2.10		
L320W80 #3											101.27		2.18		
											224.8		2.71		
											477.58		2.10		
L320W80 Curve #1	320	80	5	13	3	16	1		86.8	N/A	84.49				3%
									181.69	N/A	175.38				4%
									N/A	N/A	272.92				N/A
									416.17	N/A	407.7				2%
									509.42	N/A	529.2				-4%
L320W80 Curve #2											84.3				
											177.41				
											275.32				
											407.88				
											530.86				
L320W80 Curve #3											83.93				
											173.54				
											270.71				
											407.33				
											530.86				
L320W80 Curve #4											84.67				
											176.12				
											274.39				
											409.73				
											529.02				
L320W80 Wide 10μm								39.81	85.6	N/A	83.93	2.15			2%
								84.27	179.12	N/A	173.54	2.13			3%
								131.43	279.59	N/A	270.71	2.13			3%
								186.9	412.35	N/A	407.33	2.21			1%
								244.23	506.08	N/A	530.86	2.07			-5%
L320W80 Wide 4μm	320	80	5	13	3	16	1	43.45	97.05	N/A	N/A	2.23			
								96.94	202.15	N/A	N/A	2.09			
								203.02	444.84	N/A	N/A	2.19			

3.4.3 Temperature Dependence

The temperature coefficient of the resonance frequency (f_o) for a contour-mode rectangular plate resonator is dominated by the temperature dependencies of Young's modulus (E) and density (ρ) of the stacked material in the device layer and its dimension. A general formula of the temperature coefficient of frequency (TC_f) with a unit of ppm per degree Celsius can be expressed with an ultimately simplified form, which doesn't take the contributions of the top and bottom electrodes into account [50][51]:

$$TC_f = \frac{1}{f_o}\frac{\partial f}{\partial T} = -\frac{1}{a}\frac{\partial a}{\partial T} + \frac{1}{2}\frac{1}{E_p}\frac{\partial E_p}{\partial T} - \frac{1}{2}\frac{1}{\rho}\frac{\partial \rho}{\partial T} = -\alpha_p + \frac{1}{2}TC_E \tag{3.1}$$

where α is the fundamental geometrical parameter that sets the device resonance frequency, T is the temperature of operation, α_p is the thermal expansion coefficient of the stacked materials in the device layer and TC_E is the temperature coefficient of Young's modulus of stacked layers in the resonators.

The TC_f of this multi-layer thin-film resonator can be also determined by the temperature coefficient of Young's modulus (TC_E) of each layer by assuming that all the layers have the same area while neglecting thermal expansion contribution [52], it can be written as:

$$TC_f = \sqrt{\frac{(1+TC_{E1})E_1t_1 + (1+TC_{E2})E_2t_2 + \cdots}{E_1t_1 + E_2t_2 + \cdots}} - 1 \tag{3.2}$$

where E and t are Young's modulus and thickness of each layer, respectively.

It is essential to have a temperature insensitive and frequency stable resonator for both oscillator and filter implementations, which typically rely on the use of resonators with low frequency drift less than 20 ppm over the operating temperature range from -30 °C to +85 °C. In order to minimize the frequency variation, introducing a SiO_2 layer to structural layers of the

resonator can practically compensate TC_f since SiO_2 offers positive TC_f that is opposite to other typical materials. Other piezoelectric materials (i.e., ZnO, AlN, $LiNbO_3$) have a negative value in their temperature coefficients of elastic modulus [53]. Furthermore, the highly doped Si in the stacked resonator structural layer is helpful for the resonator fabricated on SOI wafers to reduce the temperature sensitivity of frequency [54].

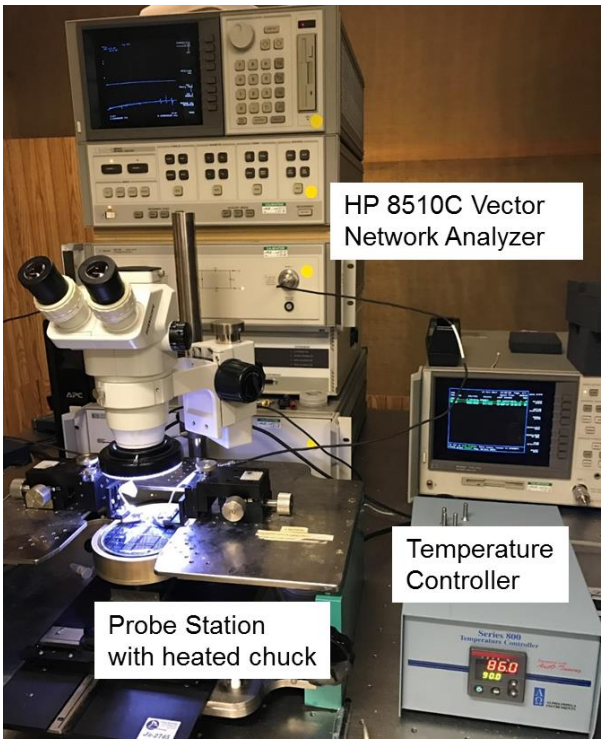


Figure 3.14 – Setup for S-parameter measurement over temperature

The TC_f of ZnO thin-film piezoelectric rectangular resonator on SOI and Diamond-on-Si are experimentally investigated and calculated from measurement results. Two-port S-parameter measurement is carried out with a setup shown in Figure 3.14 using a HP 8510C vector network analyzer, a temperature controller, and a probe station. The device wafer under test is directly heated on the chuck from 20 °C to 110 °C while the frequency response is continuously monitored and recorded. A ZnO on SOI device with body dimension of 300 μm x 91μm shown in Figure 3.15 (a) is measured to have its resonance frequency of 258 MHz at 20 °C. Its frequency response

over the temperature is displayed in Figure 3.15 (b). The resonance frequency at each temperature level is plotted. The frequency change versus temperature shows a highly linear behavior over the entire temperature range in Figure 3.15 (c). Therefore, the TC_f of a ZnO device on SOI is calculated to be -30.6 ppm/°C from the slope of the dashed line, which is similar to the measured TC_f of -31.05 ppm/ºC for the 30 µm-radius disk-shaped ZnO device on SOI as reported in [50].

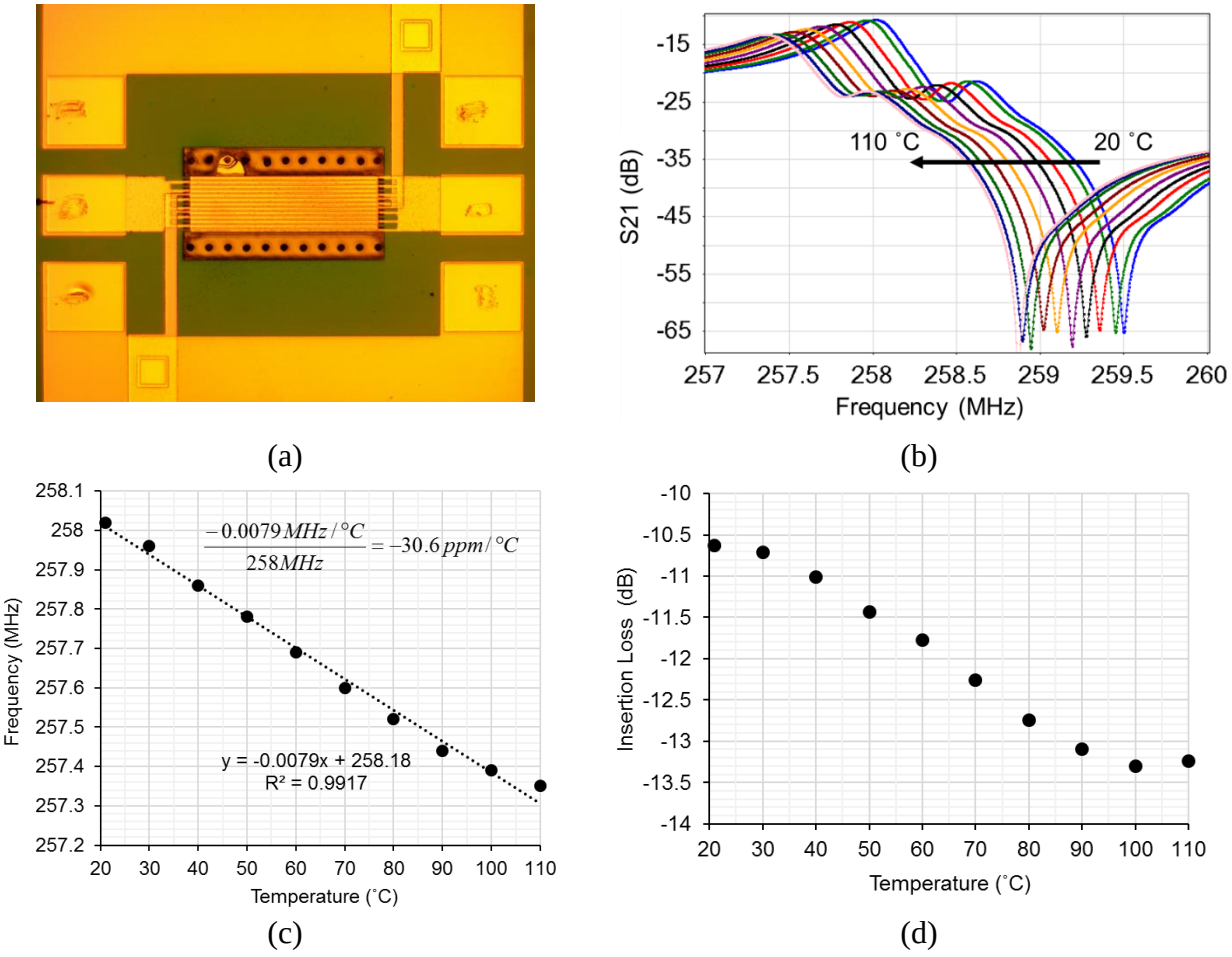


Figure 3.15 – (a) A ZnO thin-film piezoelectric rectangular resonator on SOI with its body dimension of 300 µm x 91µm, finger number of 13, finger pitch size of 7 µm, finger width of 4um and 13 pairs of tethers; (b) measured frequency response of the resonator over a temperature range from 20 to 110°C; (c) measured resonance frequency over temperature; (d) measured insertion loss of the resonance over temperature

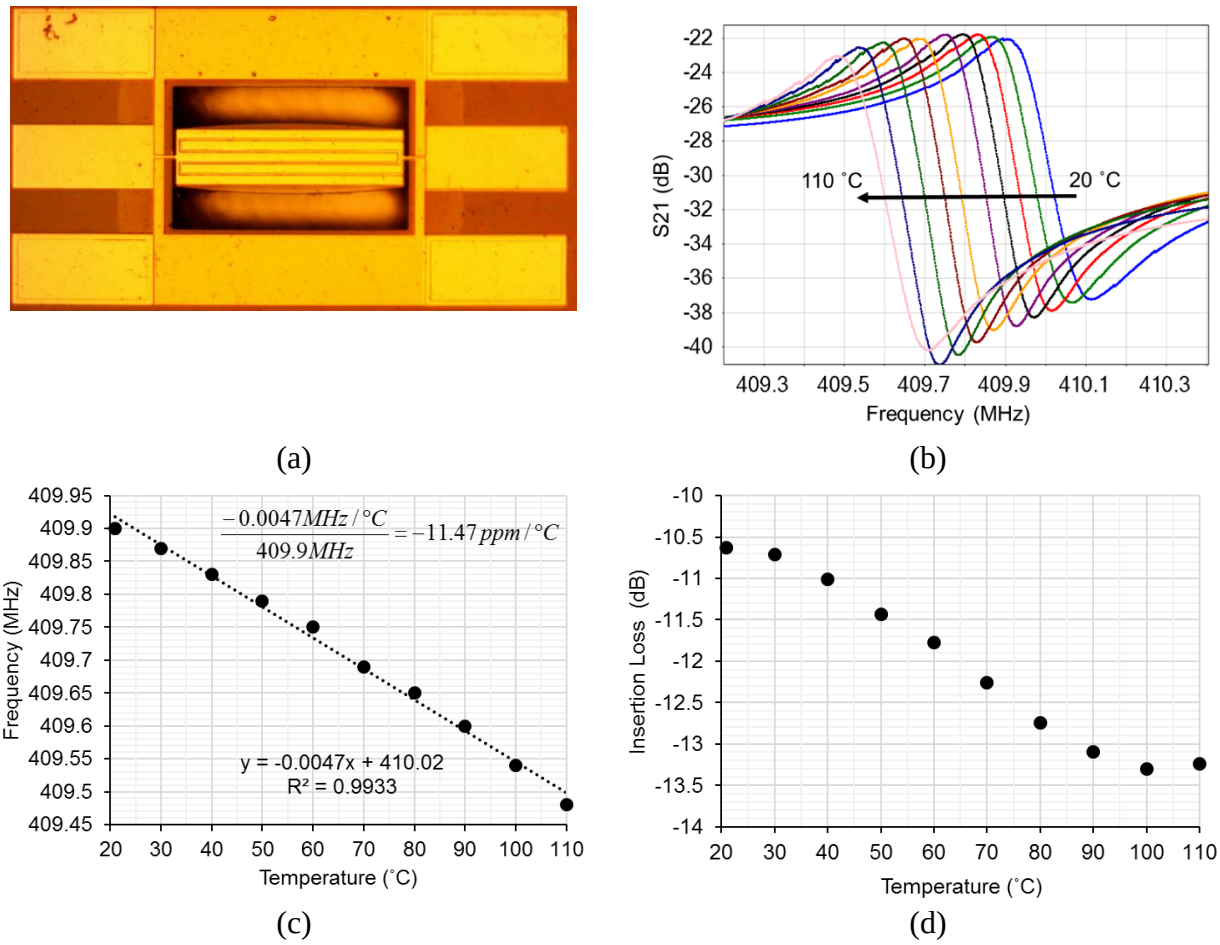


Figure 3.16 – a) A photograph of ZnO thin-film piezoelectric rectangular resonator on Diamond-on-Si with its body dimension of 320 µm x 80 µm, finger number of 5, finger pitch size of 16 µm, finger width of 13 µm and 1 pair of tethers; (b) measured frequency response of the resonator over a temperature range from 20 to 110°C; (c) measured resonance frequency over temperature; (d) measured insertion loss of the resonance over temperature

On the other hand, another ZnO device on Diamond-on-Si wafer as shown in Figure 3.16 (a) with body dimension of 320 µm x 80 µm is measured under the same condition for a direct comparison. The ZnO-on-Diamond resonator has its resonance frequency of 409.9 MHz at 20 °C. The frequency response over the temperature sweep is captured in Figure 3.16 (b). The resonance frequency at each temperature level is plotted and the best fit trend-line has a slope of -0.0047 as shown in Figure 3.16 (c). Therefore, the TC_f of a ZnO device on Diamond-on-Si is calculated to be -11.47 ppm/°C. It is obvious that the employment of thin film diamond structural layer improves

the TCF of the resonator by 18.59 ppm/°C as compared to that of a silicon device counterpart. Thus, using diamond as a part of the resonator's structural layer not only helps to boost up the quality factor but will also reduce the temperature sensitivity of the resonator. The insertion loss of the resonance peak slightly decreased with temperature as seen in Figure 3.16 (d) and Figure 3.16 (d). Additionally, the quality factor Q of the resonator is barely changed due to the temperature variations.

3.5 Circuit Model of RF Probe Pads and Microstrip Lines on Silicon-on-Insulator and Diamond-on-Silicon Substrates

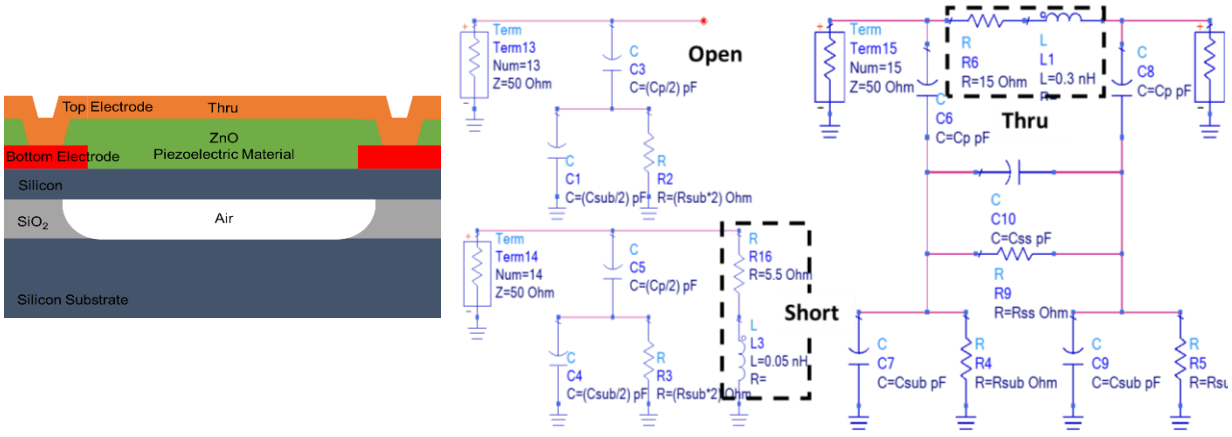
Even though the electrical behavior of a piezoelectric resonator can be perfectly represented by BVD circuit model around the operation of resonance, parasitic effects of the testing structure, which consists of a microstrip line with probe pads connection to the resonator, are not included in the circuit model for the piezoelectric resonator fabricated in-house. The RF probe pads with a 150 µm pitch in Ground-Signal-Ground (GSG) configuration are fabricated with three 200 µm x 100µm rectangular probe pads. And the microstrip line connecting electrodes of the resonator on the tethers to the probe pads are laid out long enough to ensure the probe pads are not located over the suspended area. Since most of the resonator measurements, particularly the measurements in this dissertation work, are taken with the probe tip calibration, the reference plane of the measurement is kept at the probe tip. Thus, the parasitic effects of the testing structure with substrate loss are embedded in the measurements of frequency response. One of the most accurate methods to measure the intrinsic response of a resonator is to design and implement an on-wafer multiline Thru-Reflect-Line (TRL) calibration so that the measurement reference plane can be moved to the closest point of the resonator. The other method, which is going to be investigated in this section, is to create an equivalent circuit model for the testing structure that will be manually

de-embedded from the measurement data. In this way, the parasitic elements of the testing structure can be further analyzed and understood from the basic circuit components.

For the purpose of characterization, additional three de-embedding structures (Open, Short, and Thru) are fabricated with those resonators on the same Silicon-on-Insulator and Diamond-on-Silicon wafers. An Open structure that consists of only the GSG probe pads, a Short structure formed by a 410 μm long microstrip line shorting the GSG probe pad, and a Thru structure that has a total length of 1000 μm long microstrip line including both probe pads on each side are shown in Figure 3.17 (a)-(c), respectively.

(a) (b) (c)

Figure 3.17 – Actual photographs of fabricated de-embedding structures (a) Open; (b) Short; and (c) Thru



(a) (b)

Figure 3.18 – (a) Cross-sectional view of the Thru structure; (b) equivalent circuit model of three de-embedding structures: Open, Short and Thru

Based on the physical stacks of the SOI substrate as shown in Figure 3.18 (a), a circuit schematic of all three de-embedding structures using lumped-element circuit components at microwave regime is proposed in Figure 3.18 (b) [55][56]. From the circuit representation of the Open structure, the capacitance of probe pads (C_p) is formed by the dielectric layers between the probe pads and the silicon substrate, which depends on the layer thickness, the area of the probe pads and the dielectric constant. Although the SiO_2 isolation layer is used between the probe pads and Silicon substrate, dielectric loss increases as the RF signal diverts into the substrate through SiO_2 more readily at high frequency. The resistance R_{sub} and capacitance C_{sub} describe the signal traveling path to the grounded bottom side of the wafer and they are dependent on the thickness and resistivity of the substrate. Rss and Css in the Thru circuit model explain the crosstalk through the layers between the input and output ports, which are mainly affected by the distance between the input and output ports (probe pads).

Table 3.3 – All parameters of the equivalent circuit model

	Silicon-on-Insulator (SOI)	Diamond-on-Silicon (DOS)
Cp (pF)	4	0.28
Css (pF)	5	5
Rss (kΩ)	10	10
Csub (pF)	0.054	0.018
Rsub (Ω)	325	1200

Figure 3.19 plots the frequency response of return loss and insertion loss for simulated equivalent circuit model of Open, Short and Thru in comparison with measured data on a Silicon-on-Insulator (SOI) wafer. Both the simulated S_{11} and S_{21} magnitude in dB and phase in degree match with the measurement very well for the whole frequency range from 300 kHz to 2 GHz.

The values of all the circuit components can be extracted very accurately because of such strong agreement between equivalent circuit model and actual measurement. It is obvious to note that the metal trace that shorts the probe pads plus the vias has 5.5 Ω resistive loss and 0.05 nH inductance. Additionally, the thru model suggests that 1000 μm long microstrip line with two via has 15 Ω resistance and 0.3 nH inductance. The same approach has been applied to Diamond-on-Silicon substrate and results are shown in Figure 3.20. All parameters of the equivalent circuit model are summarized in Table 3.3.

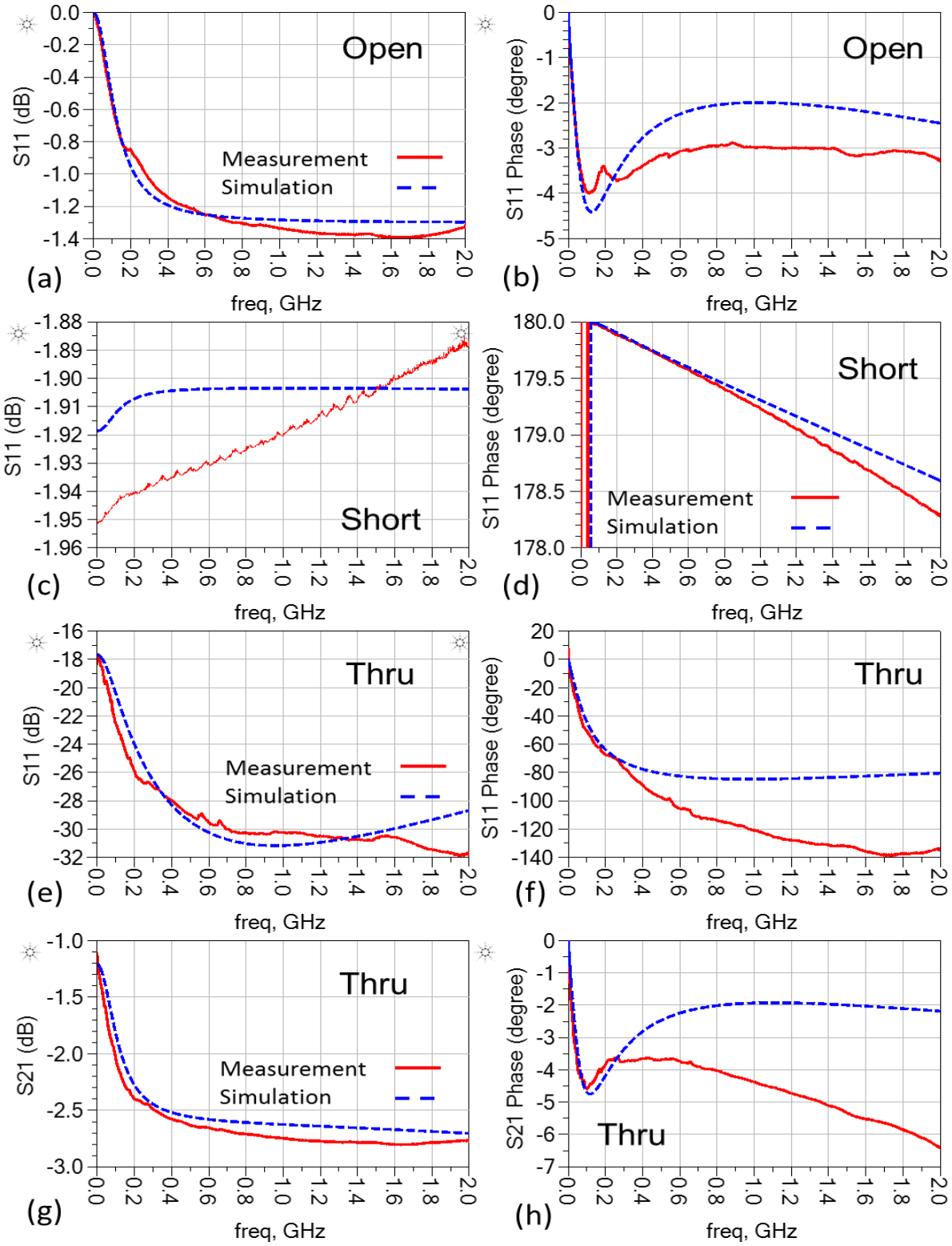


Figure 3.19 – S-parameter results of measurement versus simulation on SOI: (a) S_{11} magnitude of Open; (b) S_{11} phase of Open; (c) S_{11} magnitude of Short; (d) S_{11} phase of Short; (e) S_{11} magnitude of Thru; (f) S_{11} phase of Thru; (g) S_{21} magnitude of Thru; (h) S_{21} phase of Thru

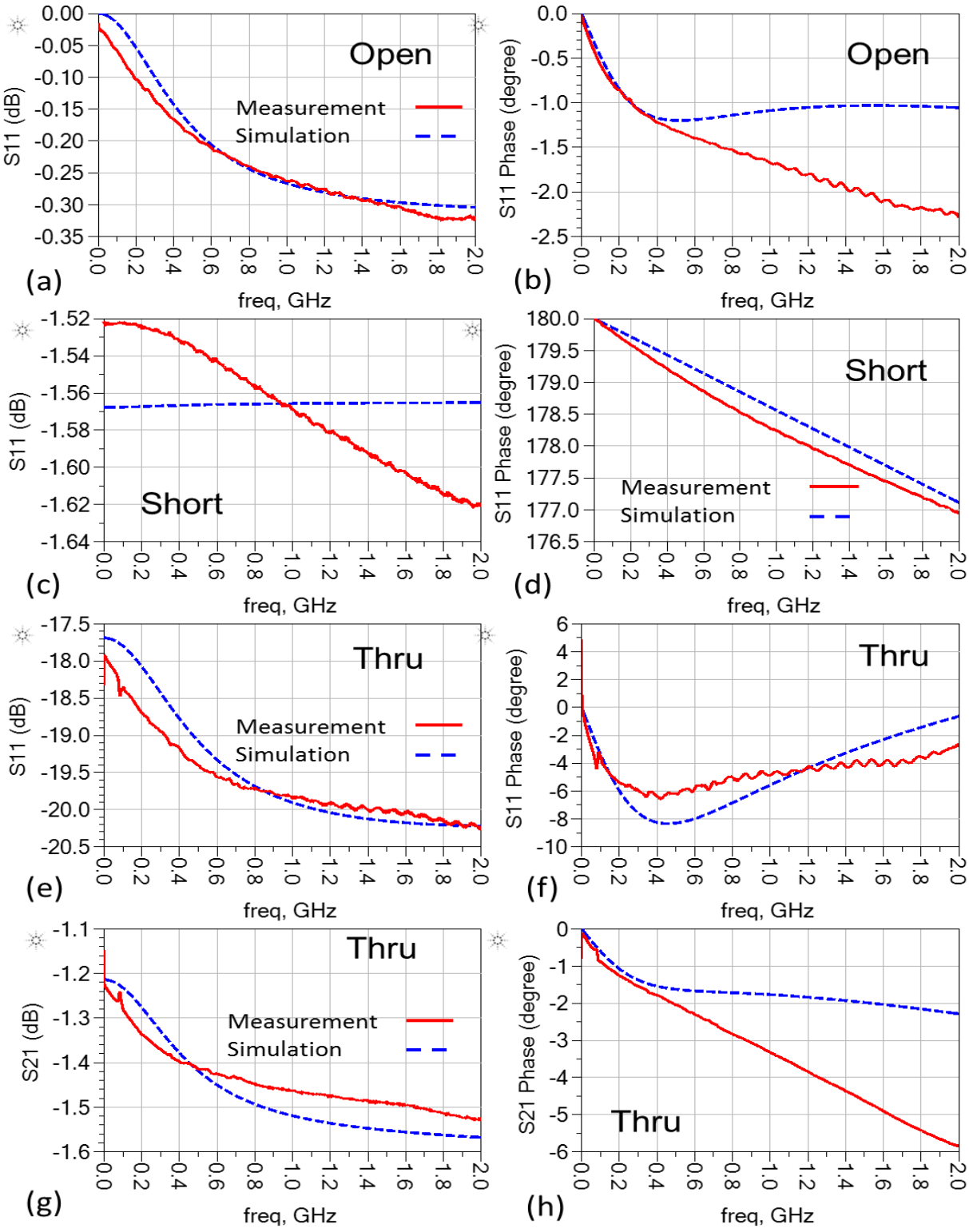


Figure 3.20 – S-parameter results of measurement vs. simulation on DOS: (a) S_{11} magnitude of Open; (b) S_{11} phase of Open; (c) S_{11} magnitude of Short; (d) S_{11} phase of Short; (e) S_{11} magnitude of Thru; (f) S_{11} phase of Thru; (g) S_{21} magnitude of Thru; (h) S_{21} phase of Thru

CHAPTER 4: MEMS-BASED OSCILLATOR DESIGN USING A ZNO-ON-SOI RESONATOR

Portions of this chapter including figures have been previously published [57]. Permissions are included in Appendix A.

In modern wireless communications, a frequency-reference oscillator is a very important frequency-setting component in any wireless transceiver systems. Traditionally, off-chip quartz crystal oscillators have been the most widely accepted choice to deliver low phase noise in the VHF range despite its low level of integration with IC's and limited frequency range up to 100MHz [58]. The advent of high-Q MEMS resonators with higher order contour modes has enabled the on-chip MEMS based oscillators to be fully integrated with IC sustaining amplifier thus exhibiting a promising low phase noise or jitter at much higher GHz frequencies than that of the quartz crystals. In the past decades, dual-mode operation principle of quartz crystal resonators have been developed to deliver highly stable reference oscillators suitable for multi-mode transceivers [59], [60]. An alternative solution by using multiple switchable MEMS resonators as a reconfigurable CMOS-MEMS oscillator has also been demonstrated [22].

In this chapter, piezoelectrically-transduced contour-mode MEMS resonators have been fabricated on a SOI wafer using the fabrication process presented in Chapter 3 and employed as on-chip frequency-setting passives, which do not require a polarization or DC bias voltage to operate, while exhibiting characteristic motional resistance typically lower than 1 kΩ under dual-mode operation. These highly-unique advantages make the piezoelectrically-transduced contour-

mode ZnO-on-SOI resonators a very promising alternative for implementation of oscillators at gigahertz frequencies.

4.1 Equivalent Electrical Circuit Model Extraction for Circuit Simulation

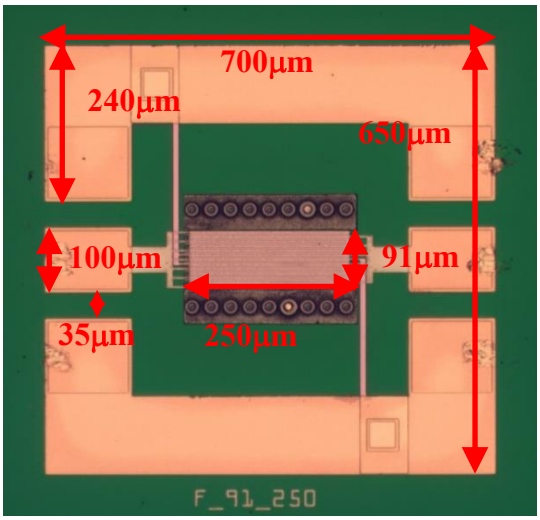


Figure 4.1 – A top-view photo of a 250 µm x 91µm ZnO-on-Si resonator along with its key dimensions that is capable of operating in two width-extensional modes

Contour-mode piezoelectrically-transduced resonators not only eliminate the need of a DC biasing voltage for their operations, but also exhibit motional impedances which typically lower than 1kΩ. This type of MEMS resonator is an excellent candidate for making frequency-reference oscillators. Figure 4.1 presents a 13th order width-extensional mode ZnO-on-SOI rectangular plate resonator with area of 250 µm × 91 µm, which has been designed to operate in two Width Extensional modes. Ground-signal-ground (GSG) probe pads for input and output terminals are designed with ground pads surrounding the resonator body to shield it. The input and output terminals are split into a total of 13 interdigitated top electrode fingers situated on top of the ZnO layer to capture the piezoelectrically transduced strain field signal. Two rows of release holes can be easily seen from the top view of the resonator as shown in Figure 4.1. Figure 4.3 (a) and (b) show the frequency response of such resonator in magnitude and phase measured using a Keysight

8753ES network analyzer. In Figure 4.3 (a), two mechanical resonances are observed at modal frequencies of 259.7 MHz and 436.4 MHz, whose harmonics are not directly overlapping with each other. The resonance at 259.7 MHz exhibits a loaded quality factor Q of 1,171.3 and an insertion loss of 9.258 dB.

A full electrical equivalent circuit model that captures both resonance modes of the ZnO-on-SOI rectangular plate resonator is developed base on the traditional series LCR model widely used for a quartz crystal. The model not only captures precise electrical behavior, but also offers sufficient insights of the ZnO-on-SOI devices. A single two-port circuit model depicted in Figure 4.2 consists of two series LCR tanks in parallel, which describe the motional resistance, inductance and capacitance of each resonance mode the resonator. The transformers in the model represent the input and output terminal of the piezoelectric transducer, where the turn ratio represents the conversion efficiency between signals in electrical and mechanical domains [61]. The feedthrough capacitor C_1 models the static capacitance of the resonator body separated by the piezoelectric ZnO material and the coupling capacitance between two ports. Pads capacitance and stray capacitance are represented by C_2, C_3, C_4 and C_5. The substrate loss R_1 is also taken into account.

The feedthrough capacitor (C_o) of the ZnO-on-SOI resonator can be extracted from S-parameter measurement data and is expressed in the Equation (4.1).

$$C_o = \frac{10^{S_{21}(dB)/20}}{2Z_o(2\pi f)} \tag{4.1}$$

Consequently, the motional capacitance (C_M), inductance (L_M), and resistance (R_M) can be evaluated from Equation (4.2-4.4) listed below:

$$C_M = C_o\left(\left(\frac{f_a}{f_s}\right)^2 - 1\right) \tag{4.2}$$

$$L_M = \frac{1}{C_M(2\pi f)^2} \tag{4.3}$$

$$R_M = 2Z_o \frac{1 - 10^{S_{21}(dB)/20}}{10^{S_{21}(dB)/20}} \tag{4.4}$$

Also, loaded quality factor (Q_L) can be evaluated from -PnB bandwidth of the resonance. Thurs, unloaded quality factor (Q_{UL}) and unloaded motional resistance (R_{UM}) can be calculated as follow.

$$Q_L = \frac{f_s}{\Delta f_{-3dB}} \tag{4.5}$$

$$Q_{UL} = Q_L(1 + \frac{2Z_o}{R_M}) \tag{4.6}$$

$$R_{UM} = \frac{R_M Q_L}{Q_{UL}} \tag{4.7}$$

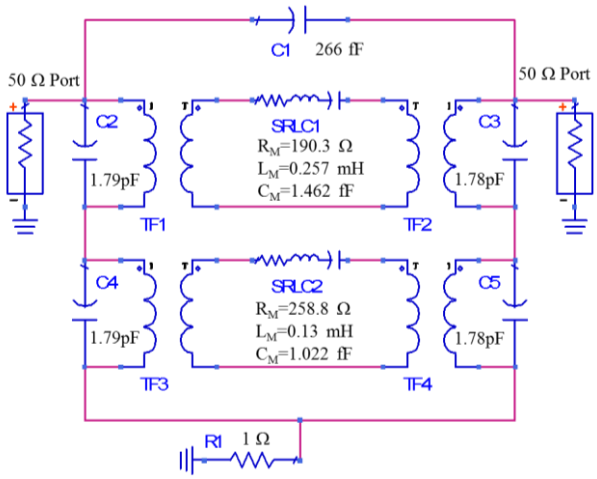


Figure 4.2 – An electrical equivalent circuit model for dual resonances of the ZnO-on-SOI resonator

Figure 4.3 (a) and (b) present the comparison between the model-predicted and measured frequency characteristics in terms of transmission amplitude and phase, respectively, which are perfectly matched across the frequency range from 200 MHz to 500 MHz.

4.2 MEMS-Based Oscillator Design

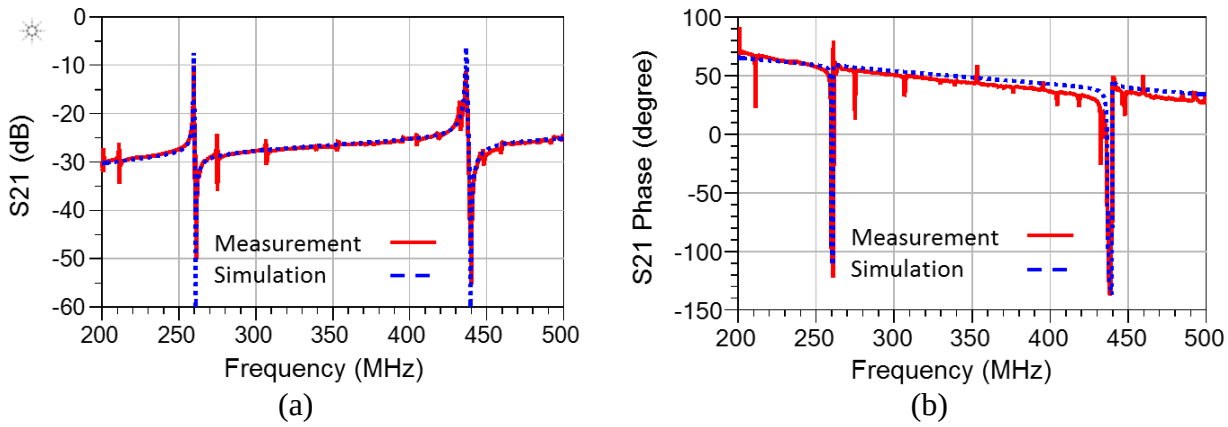


Figure 4.3 – (a) A comparison between simulated and measured frequency responses (S_{21} in dB) of the ZnO-on-SOI resonator; (b) a comparison between simulated and measured frequency responses (S_{21} in phase) of the ZnO-on-SOI resonator

Figure 4.4 depicts the oscillator block diagram. The oscillator is formed by cascading resonator and amplifier in a closed loop. The Amplifier provides enough gain and RF power for the system to sustain the oscillation, therefore it is called sustaining stage which should be stable with moderate gain while having very low noise. When the loop of the oscillator circuit is closed, the output of an oscillator can be simply viewed and captured by an oscilloscope in the time domain or a spectrum analyzer in the frequency domain.

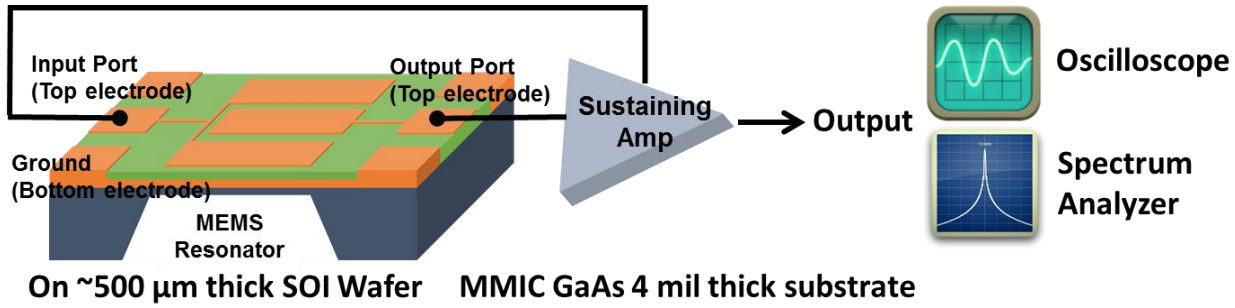


Figure 4.4 – A typical MEMS based oscillator circuit diagram

2-port open-loop analysis method is preferred for piezoelectric resonator based oscillator design because not only it can facilitate the design procedure by simulating the open-loop gain and

phase responses but also the necessary starting conditions of the oscillator can be determined from the open-loop Bode response. The oscillation condition is defined by Heinrich Georg Barkhausen and it is given in the Equation (4.8) and (4.9) for the loop gain and the loop phase conditions, respectively.

$$|A(s)\beta(s)| > 1 \tag{4.8}$$

$$\angle(A(s)\beta(s)) = n360°, n = 0,1,2 \ldots \tag{4.9}$$

Besides necessary conditions from Barkhausen's criterion, there are several additional objectives of the open-loop cascade are [29]:

- the maximum $\partial\varphi/\partial\omega$ occurs at φ_0;
- the amplifier is stable;
- the reflection coefficient (S_{11} and S_{22}) are small;
- The maximum gain margin occurs at φ_0;
- The gain margin should be moderate, typically 3 to 8 dB.

A Pierce common-source FET oscillator using the above mentioned MEMS resonator as its tank circuit has been designed through an open-loop method. To demonstrate dual-output frequencies from this oscillator, a low noise pHEMT FET (ATF-54143 from Avago Technologies) is chosen for implementing the Pierce oscillator. A complete oscillator circuit design using the model library from Modelithics is illustrated in Figure 4.5 (a) and simulated in ADS. Figure 4.5 (b) shows a simplified circuit diagram with the important design parameters specified. The open-loop gain condition for this Pierce oscillator that is related to the transconductance of the FET is particularly given by Equation (4.10) where R_E represents the equivalent resistance of the resonator and g_m is the transconductance.

$$\frac{g_m}{\omega_o R_E C_1 C_2} > 1 \tag{4.10}$$

Thus, by providing different biasing current to the FET, different oscillation frequency can be selected by the proper gain generated from the sustaining amplifier. Therefore, oscillation criterion is only strategically satisfied for one output frequency at a time.

The FET is biased with a 10.1mA of DC current so that the open-loop transmission has an 8dB gain margin to ensure the oscillation after the loop is closed. In Figure 4.5 (b) and (c), the open-loop responses in terms of both magnitude and phase from ADS simulation match the measured data very well.

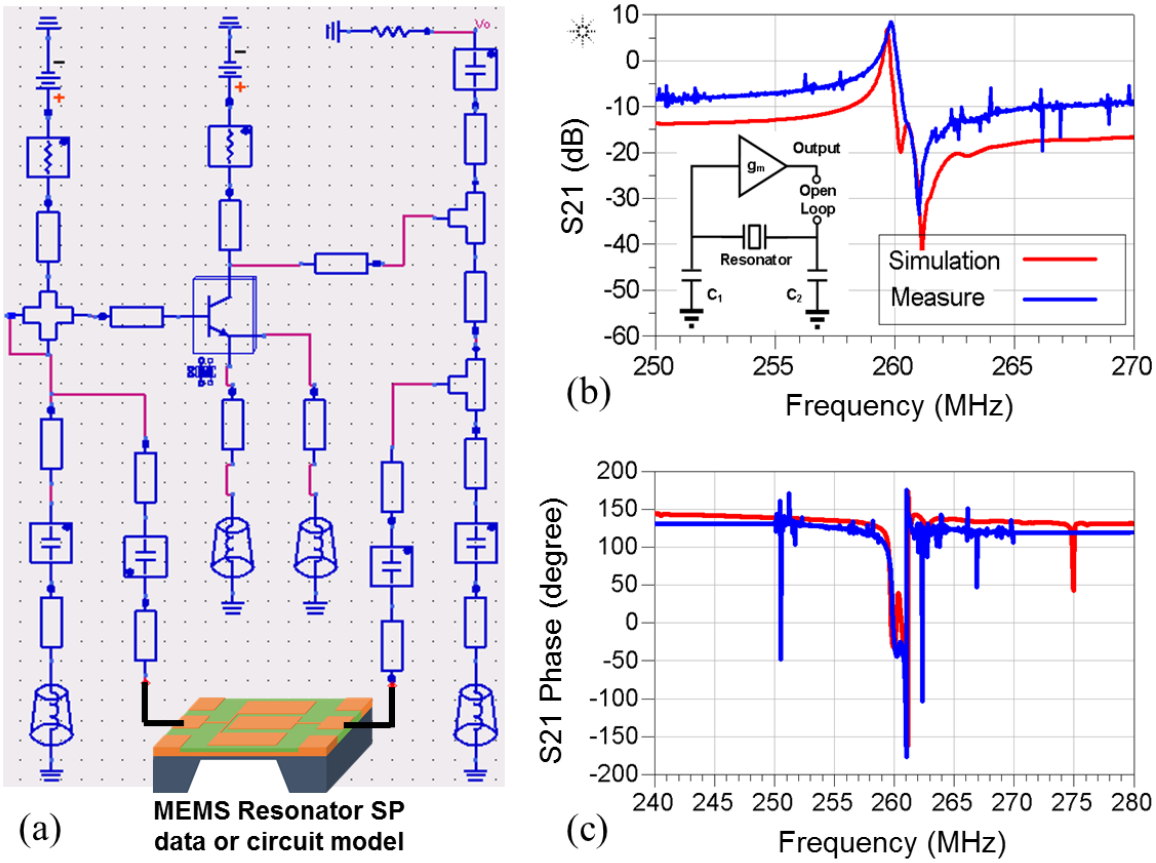
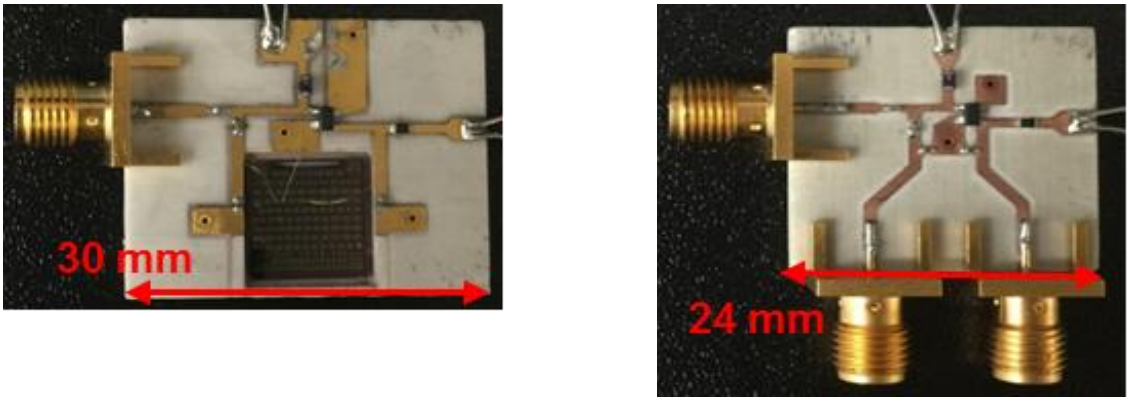


Figure 4.5 – (a) A complete Pierce oscillator circuit design simulated in ADS; (b) open-loop frequency response (S_{21} in dB) of the resonator and sustaining amplifier circuit in ADS simulation and measurement; (c) open-loop frequency response (S_{21} in phase) of the resonator and sustaining amplifier circuit in ADS simulation and measurement

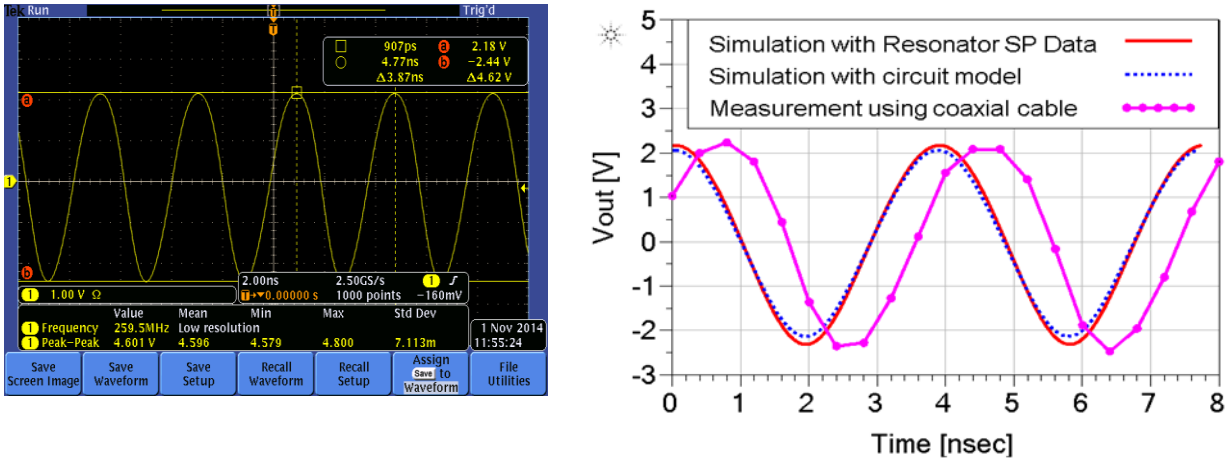
4.3 Dual-Frequency MEMS-Based Oscillator Results

Based on the aforementioned Pierce oscillator design, a sustaining amplifier is first implemented on a PCB and then integrated with ZnO-on-SOI resonators by using wire-bonding technique and coaxial connectors as shown in Figure 4.6 for the preliminary study. The coaxial connection method is designed to facilitate the assessment of multiple devices on a single resonator device die.



(a) (b)

Figure 4.6 – (a) Actual oscillator circuit milled on PCB with wire-bonded MEMS resonator; b) actual oscillator circuit milled on PCB circuit with coaxial connection to the MEMS resonator



(a) (b)

Figure 4.7 – (a) Measured time-domain response using an oscilloscope; (b) comparison between measured data and two types of simulated time-domain output waveforms

The oscillator is capable of locking into the constituent frequency of the high-*Q* MEMS resonator to produce a stable sinusoidal output waveform with a peak-to-peak amplitude of 4.62V at 259.5 MHz as shown in Figure 4.7 (a). Circuit simulation has been done using both equivalent circuit model and measured s-parameter data of the resonator. Figure 4.7 (b) compares the output waveform to two types of circuit simulation results. Both amplitude and period of the sinusoidal waveform are well comparable.

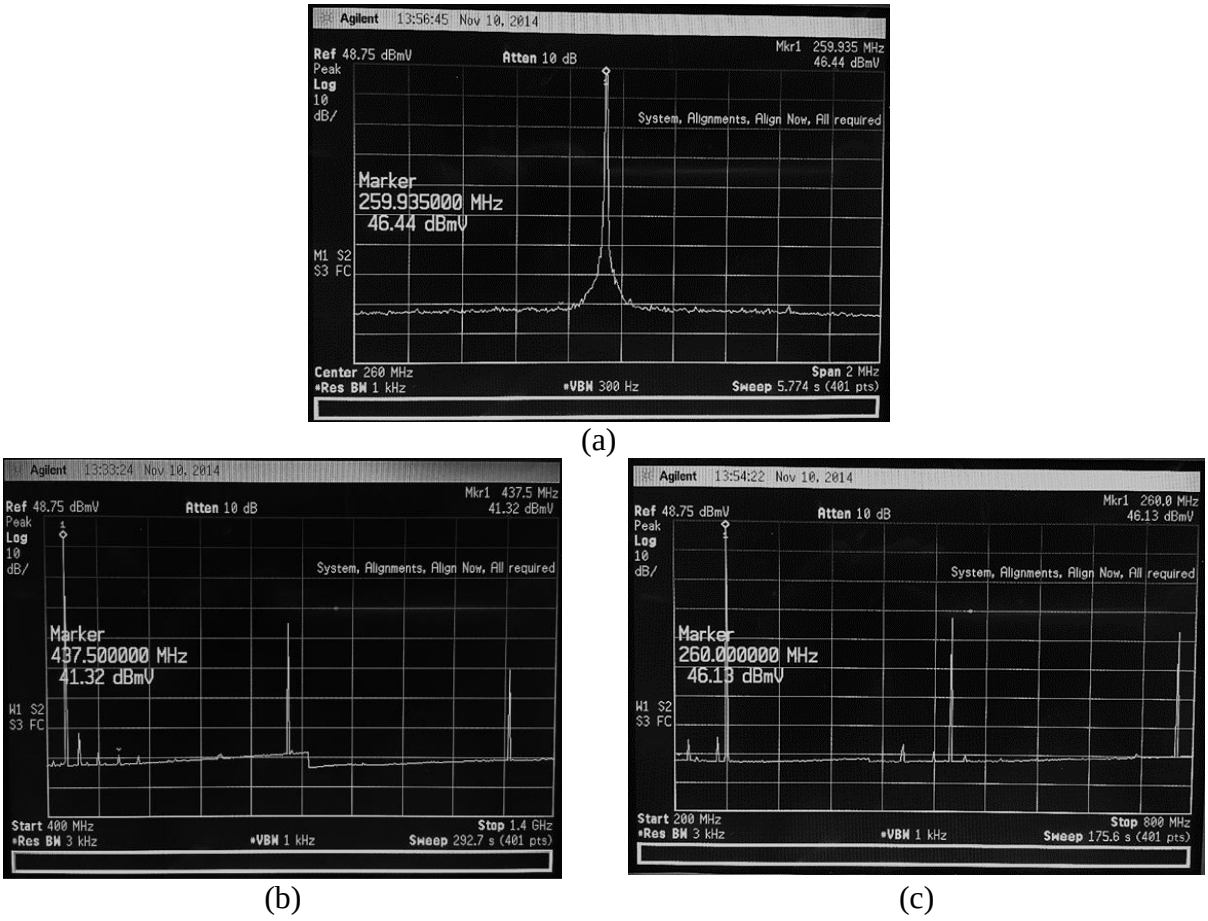


Figure 4.8 – (a) Measured frequency-domain response using a spectrum analyzer; (b) frequency spectrum of the oscillator locked to the resonant frequency of 437.5 MHz; (c) frequency spectrum of the oscillator locked to the resonant frequency of 259.5 MHz

When the sustaining amplifier is biased with 23.8 mA to result in higher g_m, the oscillator is able to oscillate at high-band frequency of 437.5 MHz that is set by the high-frequency resonance

mode. Figure 4.8 (b) shows a measured spectrum, in which the fundamental oscillation of 437.5 MHz and higher harmonics can be easily observed. Moreover, the harmonics of 259.5 MHz are not seen on the spectrum which indicates the oscillator has successfully locked to the higher resonant frequency mode at 437.5 MHz of the dual-mode ZnO-on-SOI resonator.

4.4 MEMS-Based Oscillator Phase Noise

In a transceiver block diagram, phase lock loop (PLL) is often used for down and up frequency conversion. Phase noise is crucial because it may distort the desired signal and directly affect the performance of the entire communication system. From a classical integer N PLL block diagram, the output frequency is N times of reference frequency from the oscillator. However, the penalty of such frequency multiplication lies in the raised phase noise by 20log(N). Therefore, it makes sense to have a high frequency and low phase noise oscillator for RF systems.

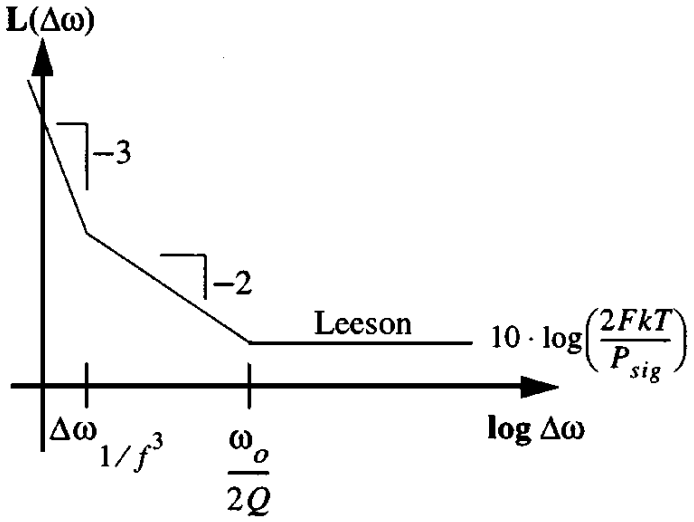
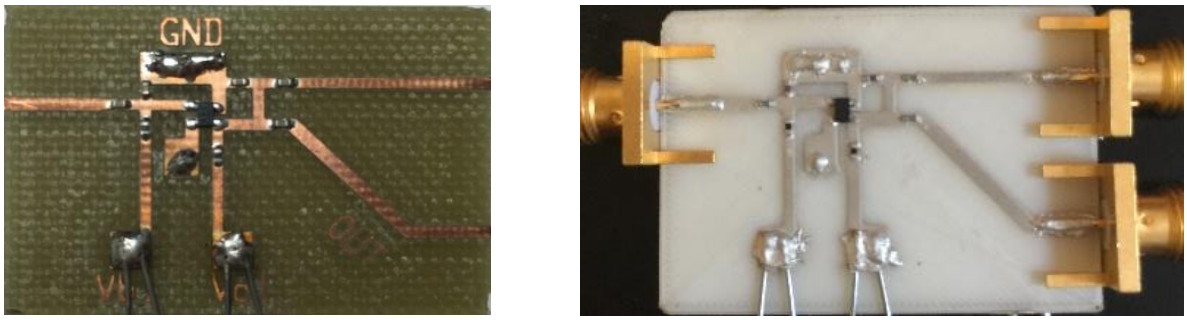


Figure 4.9 – Leeson's phase noise model

Figure 4.9 illustrates Leeson's phase noise model [62] which is the most widely used linear model for phase noise. The equation for the phase noise model of an oscillator is expressed as:

$$L(\Delta\omega) = 10log\left[\frac{2FkT}{P_{sig}} \cdot \left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \quad (4.11)$$

where F is the effective noise figure of the sustaining amplifier, k is the Boltzmann constant, T is the operating temperature, P_{sig} is the output power of the oscillator, ω_0 is the oscillation frequency of the oscillator, $\Delta\omega$ is the offset frequency at which the phase noise is measured, Q is the loaded quality factor of the resonator, and $\Delta\omega_{1/f^3}$ is the corner offset frequency. Leeson's model is empirical based on the measured noise figure and corner offset frequency. The phase noise starts to decrease at a rate of -30 dB per decade until it reaches the corner offset frequency. Then, within the half-bandwidth of the resonator (i.e., $\omega_0/2Q$), the phase noise decrease at -20 dB per decade. The far-away noise floor depends on noise figure and output amplitude of the amplifier from Equation (4.11).



(a) (b)

Figure 4.10 – (a) A MEMS based common-emitter oscillator circuit milled on PCB; (b) a 3-D printed MEMS based oscillator circuit

In order to evaluate the phase noise of the MEMS based oscillators, three oscillator circuit has been fabricated on PCB and 3-D printed ABS (Acrylonitrile Butadiene Styrene) substrate. The first one in Figure 4.10 (a) demonstrates actual circuit design on PCB using CEL SiGe HBT transistor. The second one has the identical layout using a different E-PHEMT transistor from Avago. The third one is a 3-D printed version of the first design. Two resonance frequencies at 260MHz and 430MHz of the MEMS resonator are captured depending on the designed oscillating criteria. Phase noise performance of all three configurations are measured using Agilent E5052B

Signal Source Analyzer. Figure 4.11 and Figure 4.12 present the measured phase noises of the oscillation at 260 MHz and 430 MHz, respectively. It is obvious to see the phase noise of the oscillator using SiGe HBT transistor is significantly better than using E-PHEMT at the offset frequency is less than 10 kHz due to the lower corner frequency of the HBT technology. Beyond 10 kHz, all three configurations have similar phase noise performance. It is also notable that the phase noise performance degrades as the oscillation frequency increases from 260 MHz to 430 MHz. Table 4.1 summaries the phase noise performance comparison of all three evaluation boards.

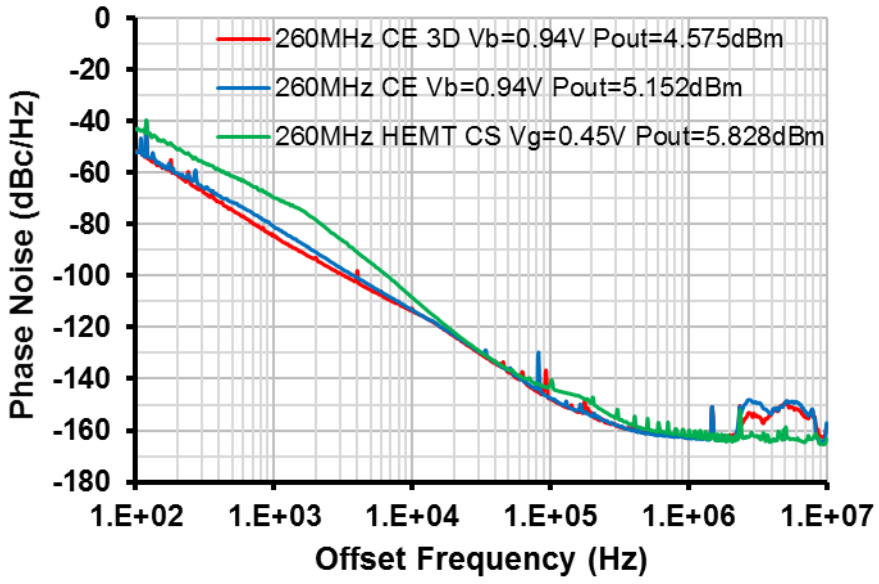


Figure 4.11 – The phase noise performance of all three oscillators at oscillation frequency of 260 MHz

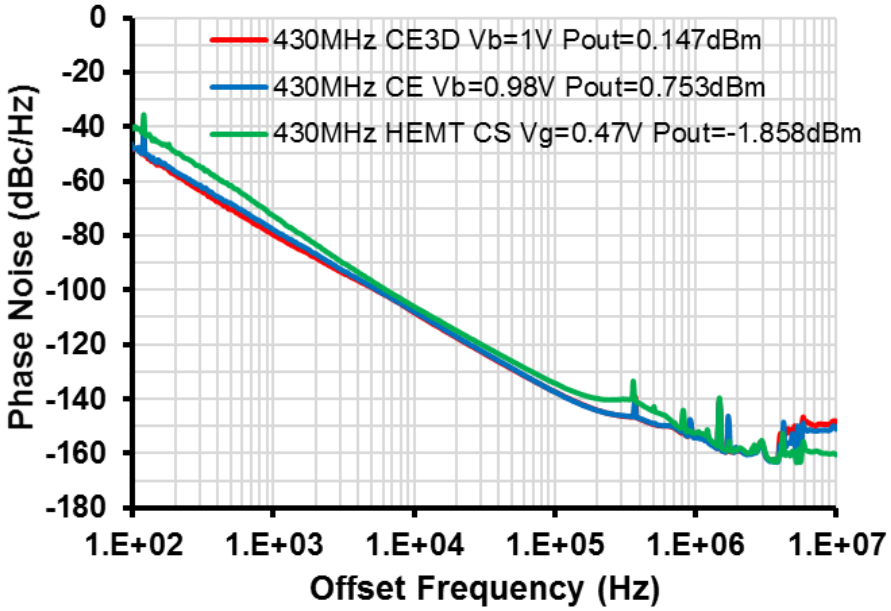


Figure 4.12 – The phase noise performance of all three oscillators at oscillation frequency of 430 MHz

Table 4.1 – Phase noise performance comparison of all three oscillators

	CEL SiGe HBT		E-PHEMT		3-D Printed CEL SiGe HBT	
Offset Frequency (Hz)	@ 260 MHz dBc/Hz	@ 430 MHz dBc/Hz	@ 260 MHz dBc/Hz	@ 430 MHz dBc/Hz	@ 260 MHz dBc/Hz	@ 430 MHz dBc/Hz
1k	-80.9	-77.8	-69.8	-72.8	-84.2	-79.8
10k	-113.1	-107.9	-108.4	-106.1	-112.5	-108.3
100k	-163.1	-154.3	-161.4	-152.4	-162.4	-154.2

CHAPTER 5: 3-D PRINTED HYBRID PACKAGING USING ADDITIVE MANUFACTURING AND LASER MACHINING

Monolithic microwave integrated circuit (MMIC) has been served as a fundamental technology for RF/microwave applications in decades and nowadays it has been massively produced for wireless, satellite communication systems and other potential high-frequency applications [62][63]. However, most of the MMICs are fabricated through semiconductor foundry service in the form of unpackaged chips [64]. Although several types of packages have been developed for MMIC integration such as SMT package [63], ceramic-based package [65], Quilt package [66] and 3-D-MMIC Wafer Level Chip Size package (WLCSP) [67], popular usage is hindered by their uniqueness, cost or fabrication complexity. Since traditional surface mount packages and wire bonds suffer from destructive parastics (in terms of frequency response) at high frequency, a great amount of research effort has been devoted to make future RF functional blocks and ICs integrated to fulfill its full potential of superior performance and enriched functionalities in a cost-effective way.

3-D Additive manufacturing (AM) has attracted a great deal of attention from the research community and rapidly grown in recent years due to the fact that numerous high-performance 3-D printed RF circuits [68-70] have been fabricated with excellent quality using 3-D printing that are on par with the circuits using printed circuit board technology. For instance, 3-D inkjet-printed interconnects for mm-Wave using coplanar waveguide transmission lines has been demonstrated [71], but the performance needs to be further improved due to the use of lossy dielectric materials.

In this chapter, a new and versatile 3-D printed multi-chip hybrid package with laser machining is developed for a mm-wave system such as a transceiver. The fabrication process for printing the interconnects laterally between ICs on a substrate is explained in detail. Laser machining technique is explored for multiple purposes in the fabrication process. Specifically, the width of 3-D printed interconnects can be accurately defined after micro-dispensing, and cavity slot for placing the IC and probe pads can be formed by laser cutting. In addition, laser trimming is studied and characterized to enhance the 3-D printing performance. S-parameters of a GaAs distributed low-noise amplifier (chip) integrated with a GaAs filter (chip) inside the hybrid package are simulated and measured from 2 to 30 GHz. The hybrid packaging also demonstrates the capability of integrating a SMT component. In the end, a 3-D printed 50 Ω microstrip line in the package with directly 3-D printed encapsulation is tested in an environmental chamber for the first time.

5.1 DPAM and Laser Machined Package Fabrication Process

An overview of the proposed direct print additive manufactured (DPAM) hybrid packaging for multiple MMICs integration is illustrated in Figure 5.1. The three main technologies that utilize the hybrid package fabrication are Fused Deposition Modeling (FDM), Micro Dispensing and Laser Machining. These tools combined together allow lateral interconnections between multiple ICs with diverse footprints, along with SMT components integrated on the same substrate. Moreover, this low-cost, low-loss, versatile integration technique can be further implemented on the integration of a wide range of subsystems fabricated with different technologies (e.g., MEMS devices on silicon, CMOS ICs, GaAs ICs, PCBs, etc.) for microwave and mm-wave applications.

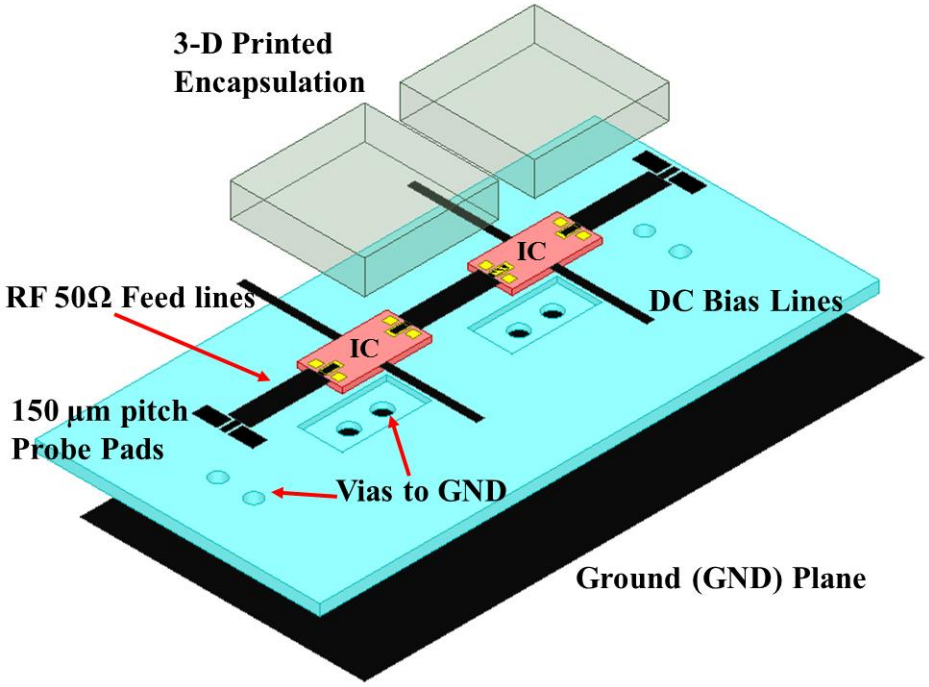


Figure 5.1 – The overall view of the proposed 3-D printed hybrid package

5.1.1 Fused Deposition of Substrate

The fabrication process of a hybrid packaging begins with the printing of a 400µm thick acrylonitrile butadiene styrene (ABS) substrate fabricated using Fused Deposition Modeling (FDM). The ABS filament is extruded through a ceramic tip at 235˚C, and deposited with designed shape on a heated metal bed kept at 110˚C. The ABS substrate is measured to have ε_r of ~ 2.1 and tanδ of ~ 0.0058 at 17 GHz [72]. In order to reduce surface roughness, four consecutive 100µm layers are printed for the desired overall thickness [73]. The ABS is chosen to be the dielectric to form the package substrate and the protective encapsulation due to its ease of printing and low cost as well as its good measured performance up to mm-wave frequencies [74].

5.1.2 Laser Trimmed RF Feedline and DC Biasing Line

Once the carrier substrate is printed, RF feedlines and DC bias connections are printed to the edge of the ICs according to the layout. DuPont CB028 conductive paste is used and micro-

dispensed with a 75 µm inner diameter ceramic tip. Once the dispensing process is complete the conductive CB028 paste is dried to maximize its conductivity at a low temperature of 90 ˚C for 60 minutes while preventing damages to the ABS substrate [75]. Although such fine printing tip can be navigated with very high precision of ± 5 µm, overspreading may occur due to the roughness of the substrate and viscosity of the conductive paste. Thus, it's necessary to trim the entire microstrip line with a laser machining not only for providing an accurate 50 Ω impedance matched RF line width but also for enhancing the RF performance (conductivity), which is going to be discussed in Chapter 5.3. Figure 5.4 (a) depicts an image of a laser trimmed microstrip line.

5.1.3 Laser Micro-Machined Cavity

In order to print the interconnects from the IC to the nearby conductive traces on the surface of the 3-D printed substrate, it is very critical to keep the surface of the chip and the surface of the printed substrate leveled due to the reason that any significant height difference can cause considerable effect on the quality and resolution of the printed interconnections. Therefore, the IC needs to be placed inside a cavity with an identical depth to compensate the thickness of the IC. A picosecond laser (Lumera Laser's SUPER RAPID-HE) is utilized to create a cavity that has the same dimensions as the IC. By programming the picosecond laser, the infrared radiation (1064 nm) scans the desired area and completely decomposes certain depth of ABS with a laser beam width of 20 um. The laser removing rate is characterized with a repetition rate of 100 kHz and various average power settings. When average power is 2.2 W, a 150 µm deep cavity is created and its cross-section profile is measured with a Dektak 150 profilometer as shown in Figure 5.2. As average power increases from 1.6 W to 2.6 W, the average cavity depth increases proportionally as can be seen in Figure 5.3, however, the boundary peak as a side effect increases as well. Figure 5.4 (b) displays an SEM image of a laser machined cavity.

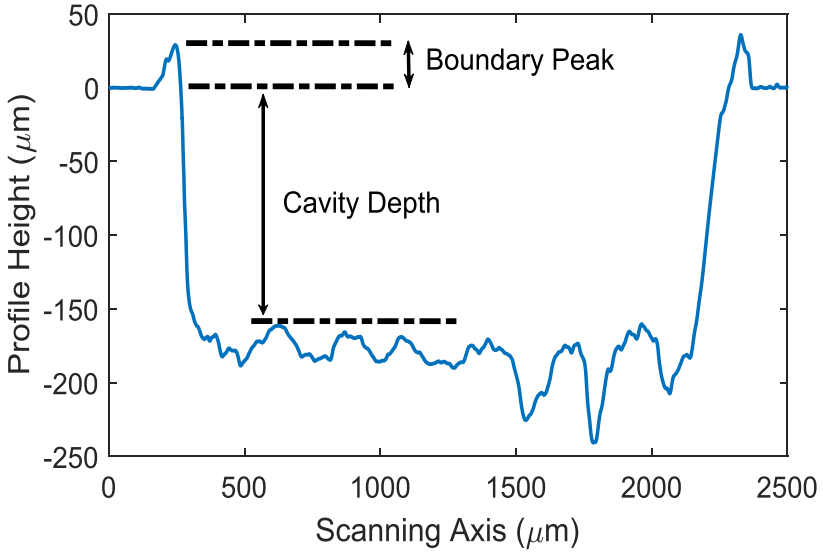


Figure 5.2 – A cross-section profile of a laser machined cavity

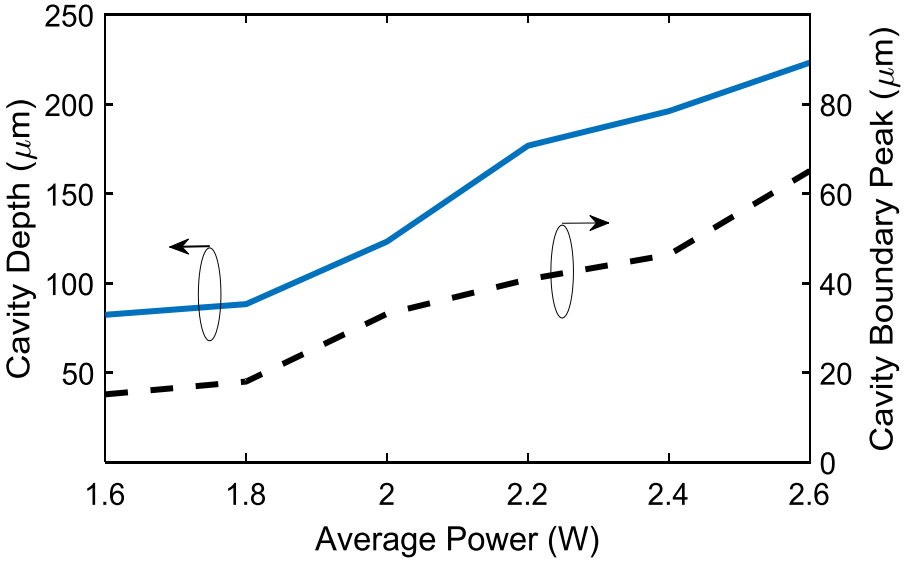


Figure 5.3 – The cavity profile with various average power levels

5.1.4 Laser Micro-Machined Probe Pads and Interconnects

At the end of input and output RF feedlines, 150 µm pitch-sized probe pads are generated by laser cutting as shown in Figure 5.4 (c). Ground pads and center signal pad are separated by a ~20 µm gap, which can be seen in the close-up picture in Figure 5.4 (d). Via holes for ground connections of both IC and probe pads shown in Figure 5.4 (e) are generated by drilling for now.

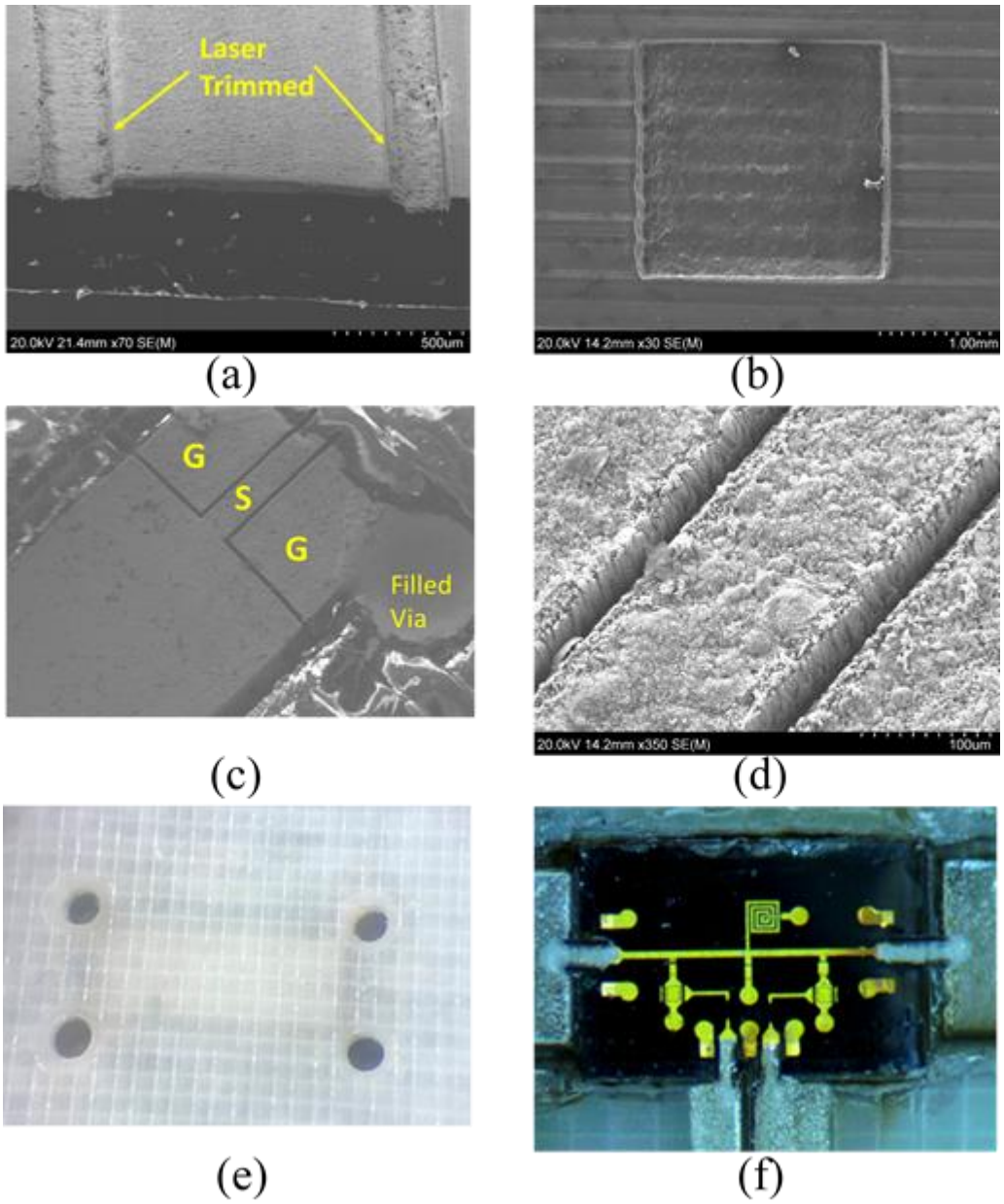


Figure 5.4 – (a) A SEM image of a laser trimmed microstrip line; b) a SEM image of a laser machined cavity; (c) a SEM image of a laser cut 150 µm pitch size probe pad; (d) a SEM picture of a close-up view of the laser cut gap; (e) via holes of the probe pads for the ground connection; (f) a hybrid packaging of a GaAs IC

They also can be implemented by 3-D printing and/or laser machining in the future. At this point, IC can be placed inside the cavity by using a non-conductive epoxy followed by printing of the interconnects. Using a printer tip with an inner diameter of 75 µm, feature sizes down to sub-hundred µm can be easily achievable when the pressure, speed and valve aperture are properly

adjusted. Figure 5.4 (f) shows a GaAs IC embedded in a 3-D printed ABS substrate with 100 µm wide interconnects, RF feedlines and DC bias lines.

5.2 Equivalent Circuit Model of 3-D Printed Probe Pads

Since all the RF measurements in this paper are taken using direct on-chip probe tip calibration, the parasitic effects of the laser cut GSG probe pads are included as a part of the measured frequency response. In order to de-embed probe pads from a DUT, an equivalent circuit model of the probe pad is developed and illustrated in the dashed box of Figure 5.5. A resistor *Rs* and inductor *Ls* connected in series represent the center signal pad and *Lp*, *Cp*, *Rp* on the parallel branch describe the via inductance, capacitance between ground pads and signal pad, and associated resistive loss, respectively.

A 3 mm long laser enhanced microstrip line as a DUT along with a 0.5 mm probing pad on each side is printed as shown in Figure 5.6 (b). Meanwhile, its full equivalent circuit model for RF simulation in Keysight Advanced Design System (ADS) is shown in Figure 5.5. All parameters of the probe pad equivalent circuit model can be extracted based on the measurement by matching the simulation and measurement results. After fitting and optimization of the circuit simulation, S-parameter S_{11} in Smith Chart and S_{21} in dB from simulation are plotted in Figure 5.6 (b) and Figure 5.7, respectively. They match very well with the measured data from 100 MHz to 35 GHz. Consequently, the following values for the parameters of the probe pad are extracted: *Rs* = 0.2 Ω, *Ls* = 0.12 nH, *Lp* = 2.25 nH, *Cp* = 0.006 pF, and *Rp* = 600 Ω. Furthermore, the microstrip line including input and output probe pads has exhibited attenuations of 0.028 dB/mm at 5 GHz, 0.187 dB/mm at 20 GHz, and 0.512 dB/mm at 30 GHz together with less than -10 dB of return loss up to 35 GHz.

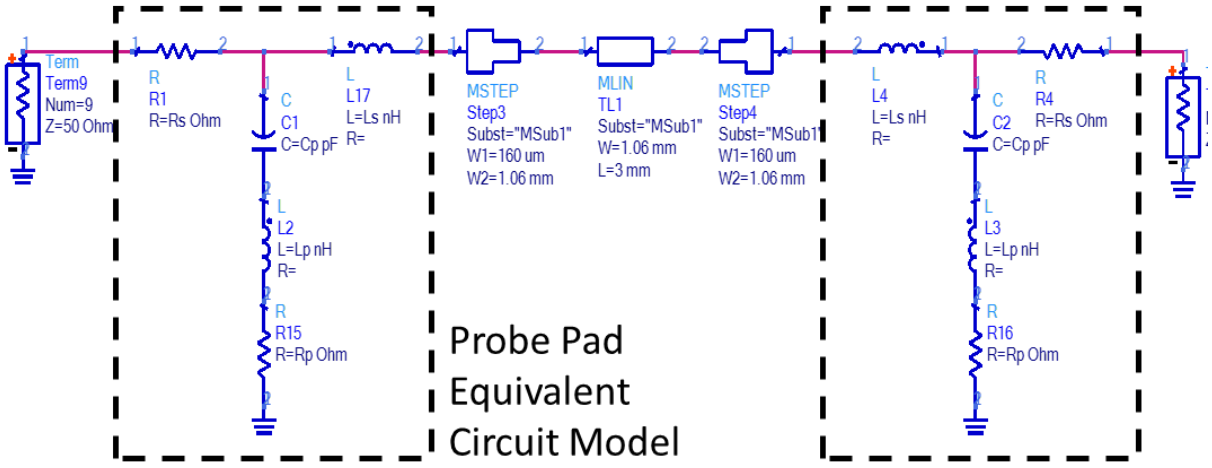
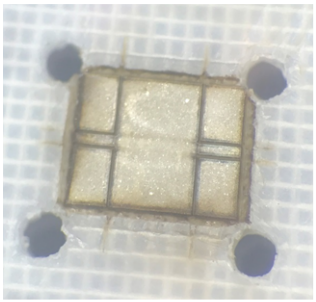
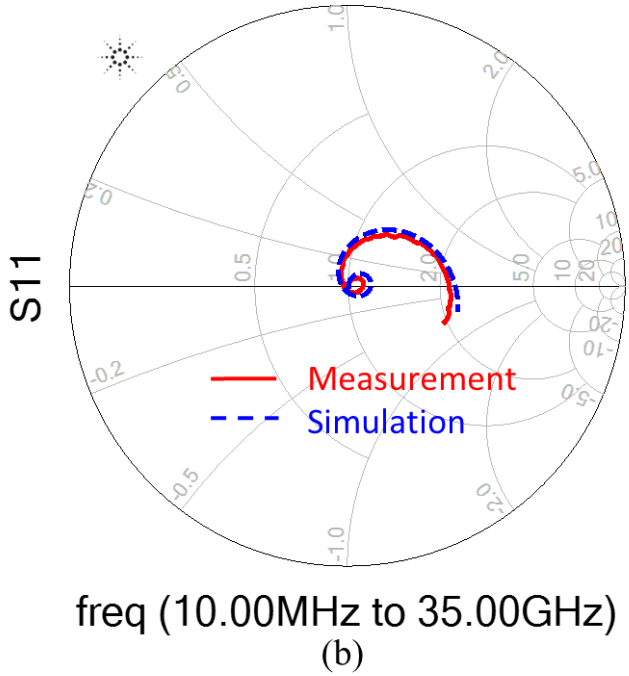


Figure 5.5 – A probe pad equivalent circuit model and a full simulation of a 3-D printed 3 mm microstrip line



(a)



(b)

Figure 5.6 – (a) A 3-D printed microstrip line and probe pads using laser machining; (b) measured and simulated frequency response S_{11} in Smith Chart of a 3-D printed 3 mm microstrip line

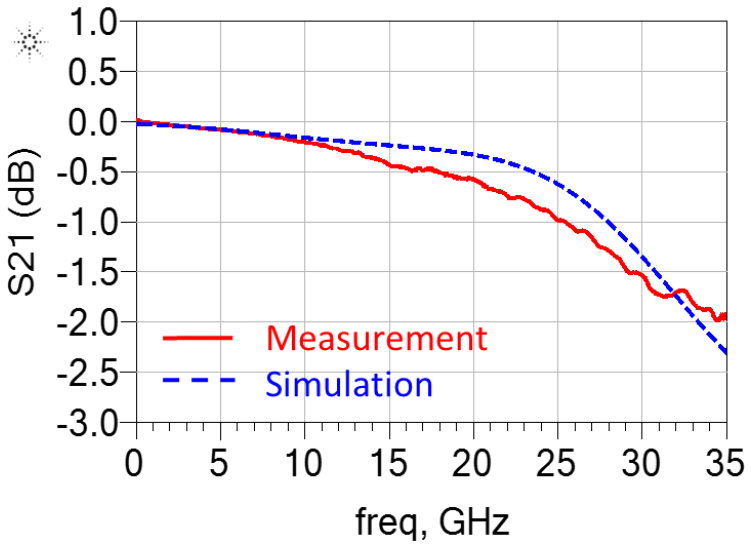


Figure 5.7 – Measured and simulated frequency response S_{21} in dB of a 3-D printed 3 mm long microstrip line

5.3 Laser Trimming Enhanced Microstrip Line

5.3.1 50 Ω Microstrip Line with Laser Trimming

Laser trimming doesn't only improve the dimensional accuracy of a printed microstrip line, but also increase RF performance. To compare with laser trimmed microstrip line fabricated in Chapter 5.2, an identical microstrip line without laser trimming is printed and measured. From measured S-parameter results of both samples plotted in Figure 5.8 and 5.9, it can be readily seen that laser trimmed microstrip has shown significantly better return loss for the entire frequency range. More importantly, the laser trimming has led to significant improvement of the insertion loss by 0.061 dB at 5 GHz, 0.918 dB at 20 GHz and 0.727 dB at 30 GHz. It's also easy to notice that the probe pad brings considerable impact to overall RF performance by comparing the results with and without applying the de-embedding technique, especially at higher frequency. After de-embedding, laser trimmed microstrip line only has a insertion loss of 0.077 dB at 5 GHz, 0.554 dB at 20 GHz and 0.962 dB at 30 GHz that are corresponding to a propagation loss of 0.026 dB/mm, 0.185 dB/mm and 0.321 dB/mm, respectively.

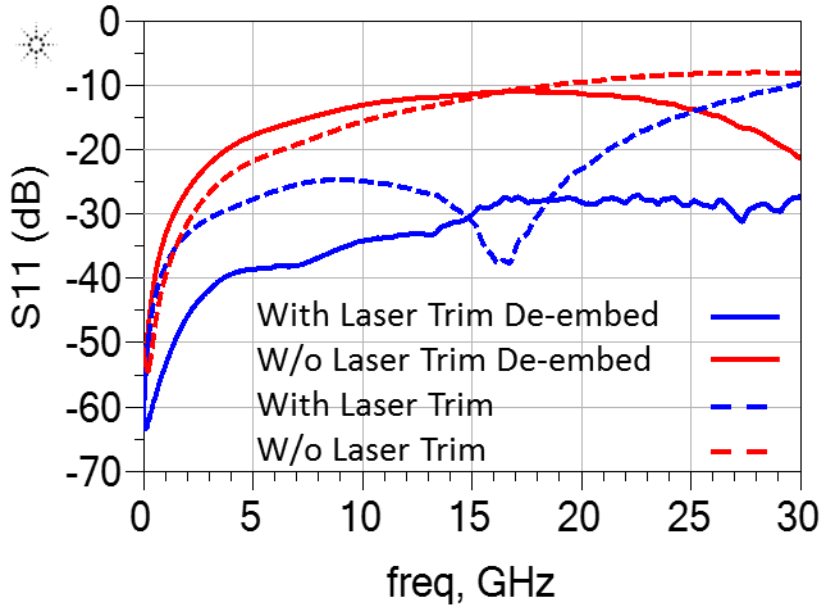


Figure 5.8 – Measured frequency response S_{11} in dB of a 3 mm microstrip line with laser trimming, without laser trimming, with laser trimming after de-embedding and without laser trimming after de-embedding

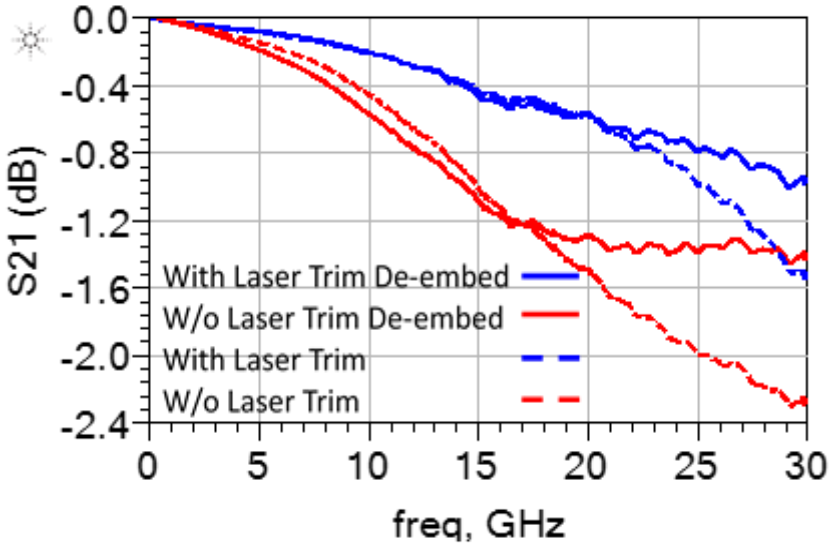


Figure 5.9 – Measured frequency response S_{21} in dB of a 3 mm microstrip line with laser trimming, without laser trimming, with laser trimming after de-embedding and without laser trimming after de-embedding

5.3.2 Propagation Constant Calculation

The propagation constant is defined as $\gamma = \alpha + j\beta$, where α is the attenuation constant, and β is the phase constant. In this work, γ is computed from the measured S-parameters, using the

expressions described in [76]. The propagation for the 50 Ω microstrip line described in the previous subsection is computed, and the results for the attenuation constant (α) and phased constant (β) are shown in Figure 5.10 (a) and (b), respectively. It is observed that the attenuation of the printed microstrip line is reduced by around 30% at 30 GHz due to the laser trimming. This loss reduction due to the laser processing is expected since it improves the edge roughness of the conductive layer, and there is a solidification of the silver particles that occur at the edges of the laser machined conductive layer as described in [77]. The phase constant of the laser trimmed microstrip line in Figure 5.10 (b) shows a reduction of around 8% at 30 GHz, when compared to the printed microstrip line without laser trimming. This can be ascribed to the overall edge roughness reduction.

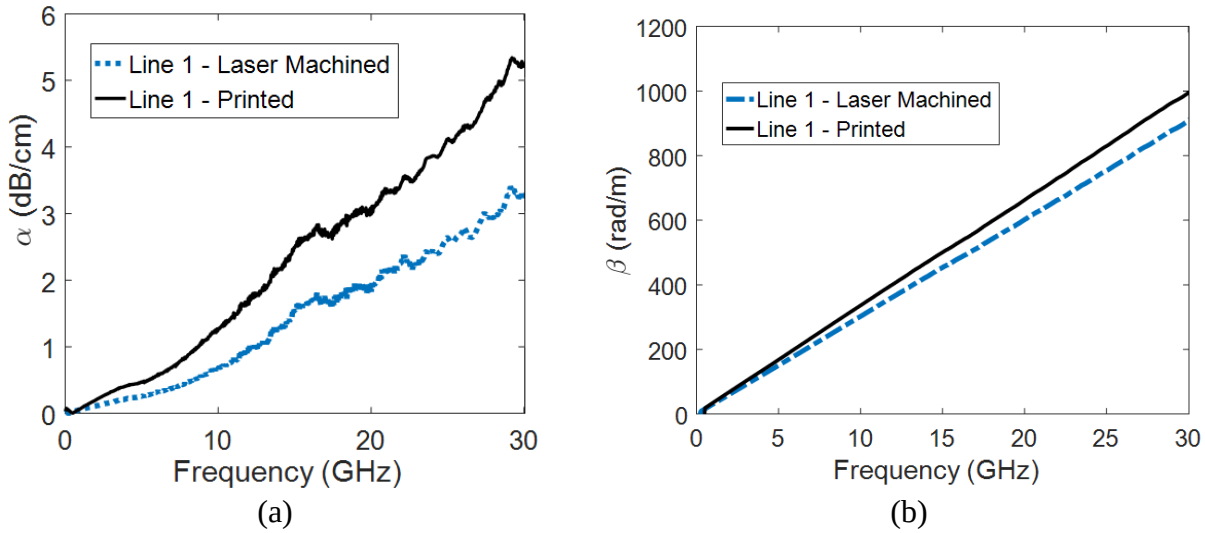


Figure 5.10 – (a) Attenuation constant; and (b) phased constant of a 3 mm laser trimmed microstrip line after de-embedding in comparison to a microstrip line without laser trimming

5.4 3-D Printed Hybrid Packaging

For the purpose of demonstrating the effectiveness and feasibility of 3-D printed interconnects and hybrid packaging, a GaAs chip with a newly designed distributed low-noise

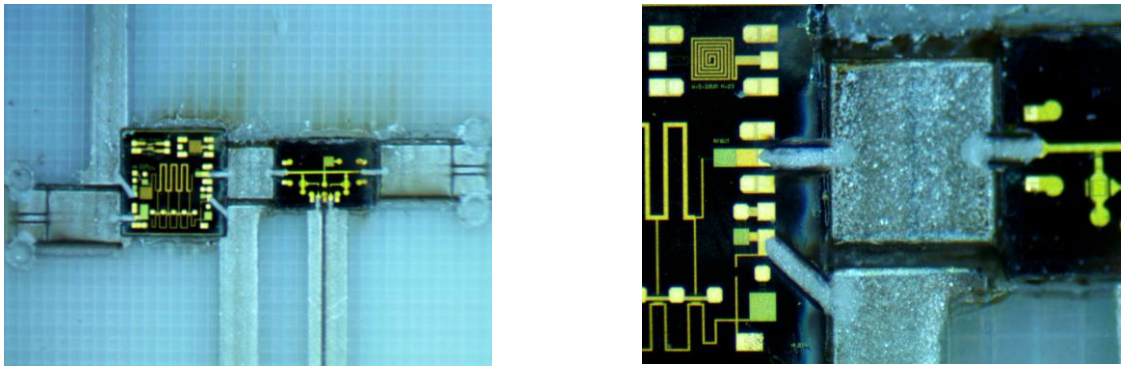
amplifier is successfully integrated with a GaAs transistor based tunable bandpass filter by using an additive manufactured substrate. The design specifications of the amplifier IC, filter IC, integrated package and measurements are described in the following section. In addition, a typical 0201 surface-mount technology (SMT) lumped component is also assembled inside the substrate to demonstrate the 3-D printed integration capability of the proposed hybrid packaging technique.

5.4.1 Integration of Multiple ICs

A distributed LNA (DLNA) fabricated by the Qorvo's foundry service using their 0.5 μm GaAs substrate E/D-mode (Enhancement and Depletion mode) pHEMT (pseudomorphic high-electron-mobility-transistor) technology has a dimension of 1.8 x 1.5 x 0.1 mm^3. This DLNA based on the traveling wave concept included four-stage cascade together to provide a flat gain of 11 dB with ±0.5 dB ripple from 2 to 22 GHz as shown in Figure 5.13 (blue). The modified gate-line impedance technique is used to reduce noise figure [78] as well as drain-line impedance thus improving the gain flatness and return loss. The length of parallel transmission lines at input and output are optimized based on the design guidelines from [79] and techniques in [80] so the LNA achieves a VSWR of 1.8 for both input and output while exhibiting only 2.6 dB mid-band noise figure. The transistor-based tunable filter is also fabricated on GaAs substrate with a size of 1.8 x 1 x 0.1 mm^3. When a bias voltage of -10 V is applied, the filter is designed to have passband center frequency at 5 GHz. Figure 5.12 (red) shows the filter response with a return loss less than -20 dB at 5 GHz and Figure 5.13 (red) shows an insertion loss of 0.52 dB for the passband of the filter.

Figure 5.11 (a) shows a complete hybrid package of a DLNA (chip) cascaded with the filter (chip) on a plastic 3-D printed ABS substrate using 50 Ω microstrip line as RF feed lines and transition between the two IC chips. Probe pads and necessary DC bias lines are also printed as

well for the measurement purpose. Figure 5.11 (b) presents a close-up view of the transition line, which consists of a 1 mm 50 Ω microstrip line and two 100 µm wide interconnects.



(a) (b)

Figure 5.11 – (a) Actual hybrid package of a GaAs distributed LNA and a GaAs active band-pass filter; (b) a close-up view of the transition and interconnects between ICs

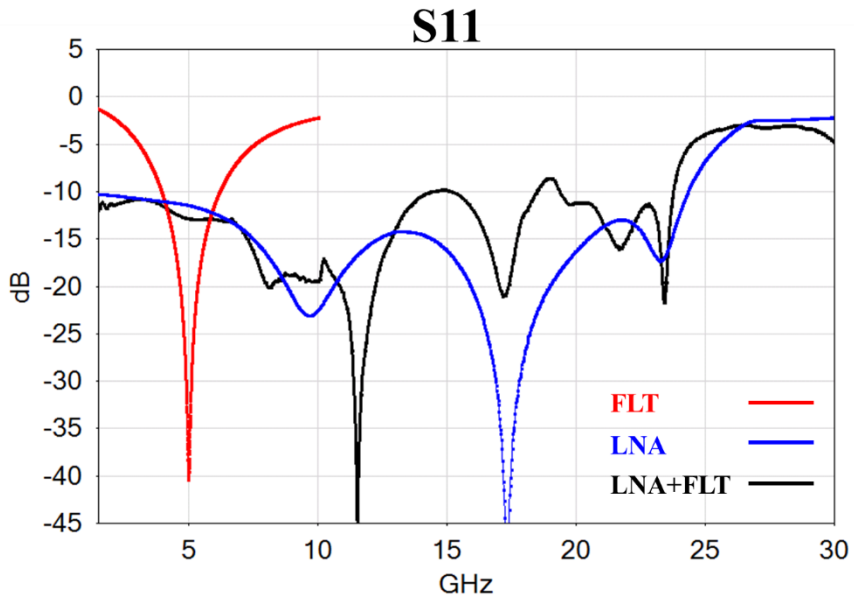


Figure 5.12 – Measured frequency response S_{11} in dB of a stand-alone filter, a stand-alone low-noise amplifier and both ICs in cascade

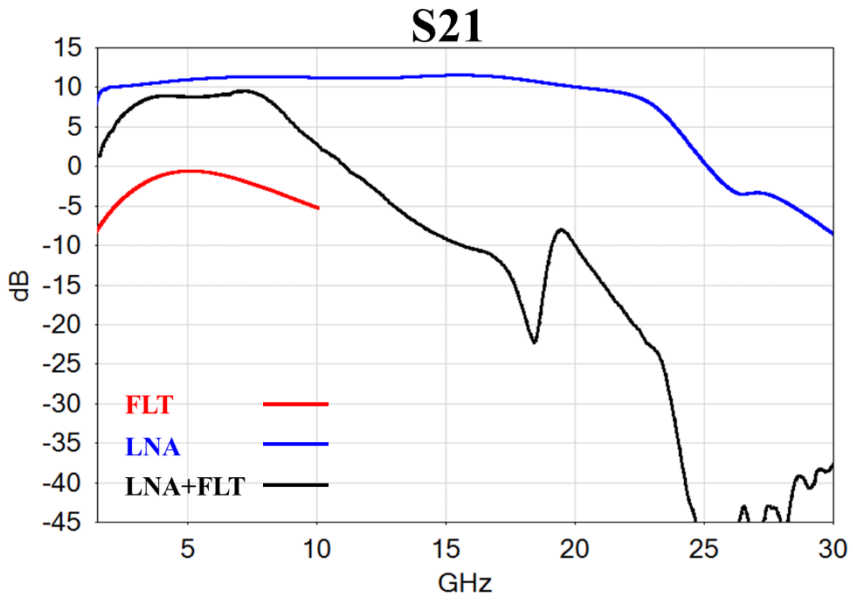


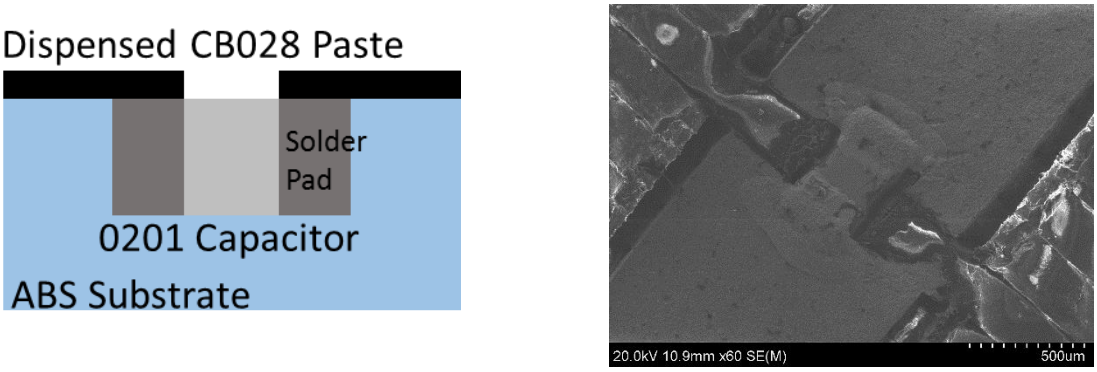
Figure 5.13 – Measured frequency response S_{21} in dB of a stand-alone filter, a stand-alone low-noise amplifier and both ICs in cascade

Figure 5.12 and 5.13 plots the measured S-parameter S_{11} and S_{21} in dB of the stand-alone GaAs Filter in red, the stand-alone GaAs DLNA in blue and both ICs in a serially cascaded configuration in black, respectively. It can be seen that the input return loss of the integrated package is still less than -10 dB within the operating frequency, thus there is fairly low impedance mismatch from the printed RF input feedline and the interconnect. The insertion loss of the 3-D printed overall package which includes 3 mm RF feed lines, 1mm transition line between ICs and all the interconnects from ICs' signal pads is only 0.21 dB at 7 GHz.

5.4.2 Integration of Surface-Mount Technology (SMT) Components

Not only IC chips can be integrated together in a hybrid package using the standard fabrication procedure described in the prior section, but also SMT component can be easily buried inside the substrate with the interconnect on the top of the component. Figure 5.14 (a) illustrates the cross-section of the SMT package. A size of 0201 10 nF SMT capacitor from AVX is assembled inside a 400μm thick ABS substrate in Figure 5.14 (b). First, a cavity that has the same dimensions of the SMT capacitor is formed using laser machining. Then, 1 mm 50 Ω RF feedlines

with the probe pads are printed and connected to the contacting pads of the capacitor on each side. The frequency response of such capacitor is measured up to 40 GHz. Using the probe pad equivalent circuit model and the Modelthics Microwave Global Models™ of this capacitor, a full circuit model of the capacitor in the package is created and simulated in ADS as shown in Figure 5.15. The S-Parameters of both simulated and measured results are plotted in Figure 5.16 and 5.17. Both S_{11} and S_{21} have shown great agreements between measurement and simulation throughout the entire operating frequency.



(a) (b)

Figure 5.14 – (a) A cross-section view of a SMT 0201 capacitor in the 3-D printed hybrid package; b) a SEM image of an integrated 0201 capacitor

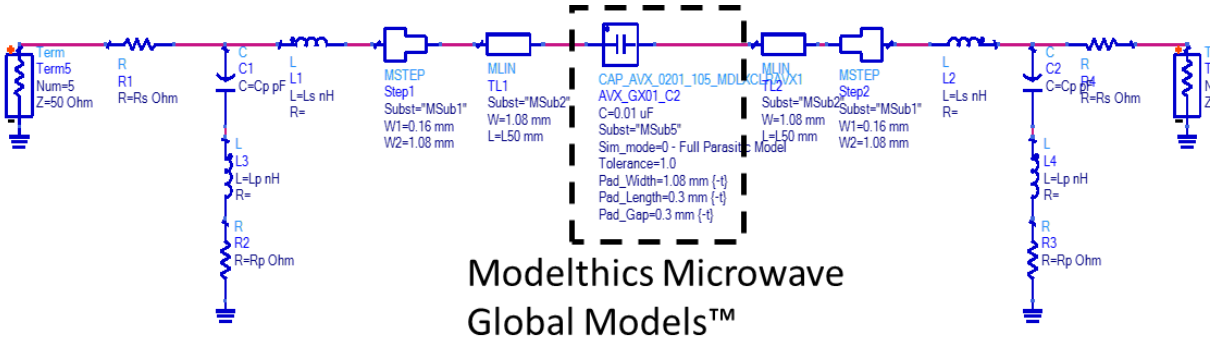


Figure 5.15 – A full equivalent circuit model of the 3-D printed 0201 capacitor with probe pads

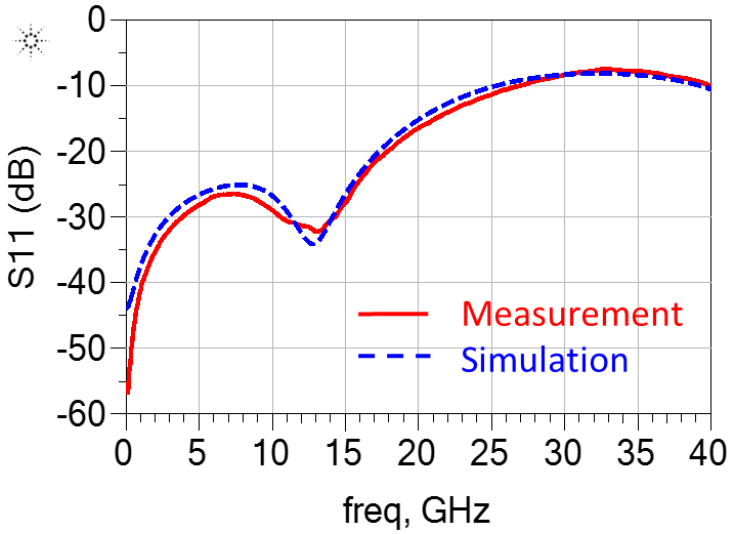


Figure 5.16 – Measured and simulated frequency response S_{11} in dB of the 3-D printed 0201 capacitor

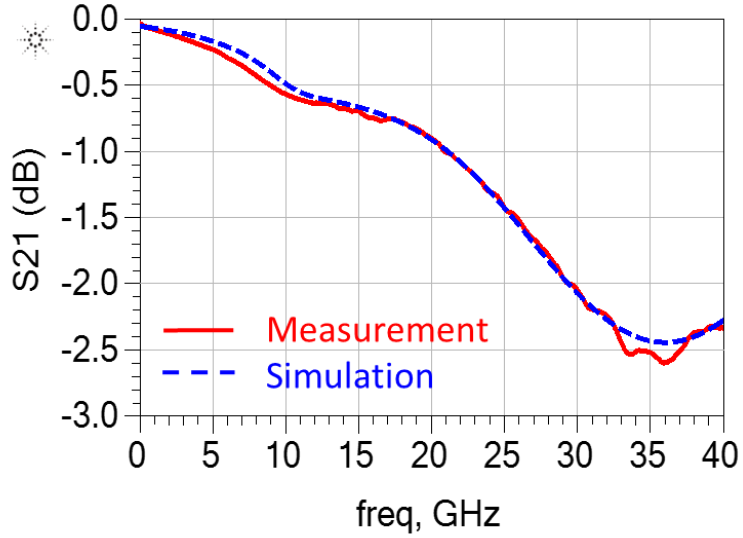


Figure 5.17 – Measured and simulated frequency response S_{21} in dB of the 3-D printed 0201 capacitor

5.5 Humidity and Temperature Cycling

It is essential to study the RF characteristics of a 3-D printed ABS substrate with the encapsulation as a complete package. The RF performance of the plastic package is impacted by the environmental conditions such as humidity and temperature. In this section, how ABS as the main material of a hybrid package behaves in different humidity level and temperature is explored

and studied for the first time. To conduct this study, a laser trimmed 50 Ω microstrip line on a 400 μm thick ABS substrate shown in Figure 5.18 (a) is fabricated with a hollow IC encapsulation printed on the top. In prior work [81], it has been proven that the encapsulation shows no RF response impact to the device underneath. A k-type end launch SMA connector is used at the edge of the printed sample for S-parameter measurement inside an environmental chamber.

Figure 5.18 (c) shows the test setup using a N5227A PNA Microwave Network Analyzer from Keysight and an environmental test chamber from Cincinnati Sub-Zero. The DUT is placed and measured inside the chamber for 20 hours after the humidity level of the chamber is switched from 40% to 100%. The insert loss of the microstrip line is captured over the time and the results are plotted in Figure 5.19 (a). The data in wetting period suggests the ABS absorbs water moisture slowly with time, which raises the insertion loss dramatically from ~2 dB to ~17 dB at 30 GHz in 1200 minutes. Once insertion loss of wet sample is saturated, the humidity level is set back to 40%, the frequency response of the microstrip line during this drying process is recorded. It is seen that the frequency response of the microstrip recovers back to original status in 10 hours.

When the temperature changes from 25 to 80 ˚C in the chamber while the humidity is fixed at 40%, the insertion loss increases accordingly at 8 GHz and 32 GHz as shown in Figure 5.19 (b). Thus, it is experimentally observed that overall loss increases due to the increasing temperature of the ABS substrate. Since the ABS package shows no water resistance ability from the humidity test, Parylene N film is also explored to coat on the surface of the entire package so that water moisture can't penetrate into ABS package. Fig. 9 (b) shows a sample is successfully covered by the Parylene N film for water resistance.

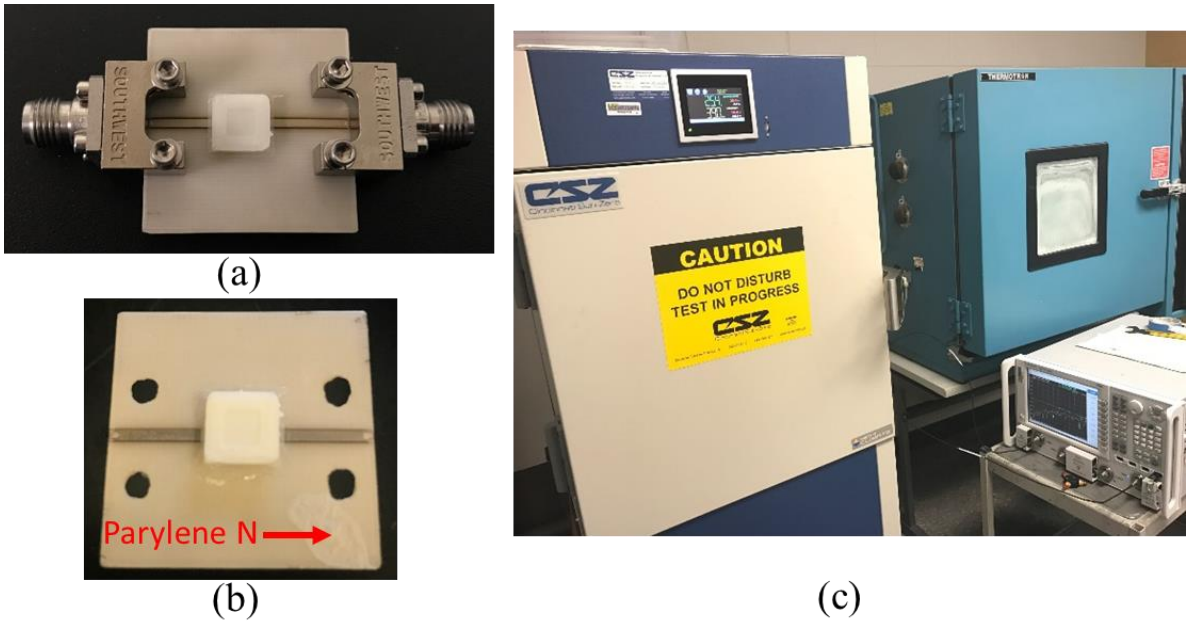


Figure 5.18 – (a) A 3-D printed 50 Ω microstrip line with a hollow encapsulation on top as a DUT for humidity and temperature cycling test; (b) the DUT coated with Parylene N for water resist; (c) humidity and temperature cycling test setup with an environmental test chamber and a PNA

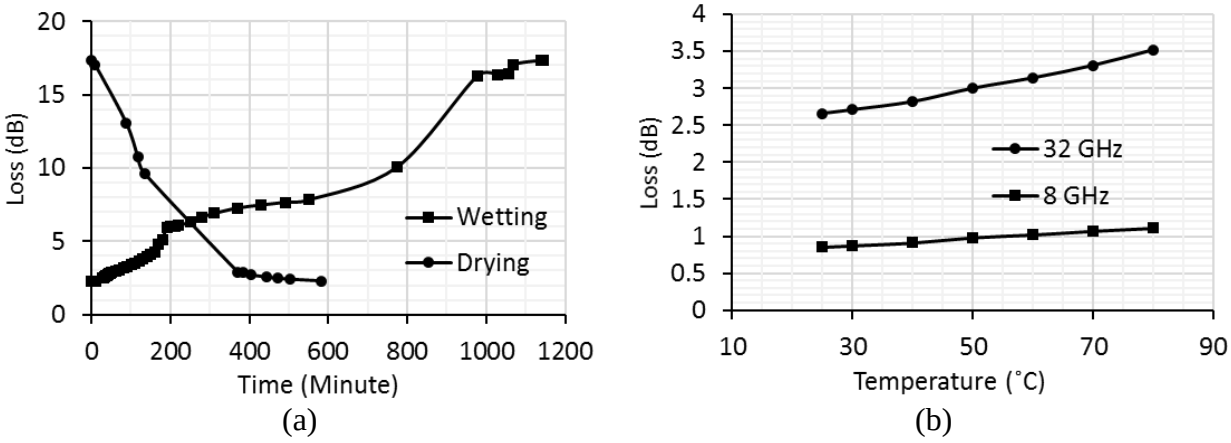


Figure 5.19 – (a) Loss of the 3-D printed microstrip line over time during drying and wetting process; (b) loss of the 3-D printed microstrip line vs. temperature changing from 25 to 80 ˚C

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this dissertation, three main topics have been investigated that are closely related and sequentially depended on each other. First, design, micro-fabrication, simulation, testing and modeling of piezoelectrically-transduced MEMS resonators have been thoroughly studied and implemented. Micro-fabrication of designed devices has been done successfully at the Nanotechnology Research & Education Center (NREC) at University of South Florida based on in-house developed fabrication processes. The on-wafer testing of those devices shows very promising results and validates the design concepts at the same time. ZnO disk contour mode resonator demonstrates a fairly low feedthrough level of -50 dB and a reasonably high quality factor (*Q*) of 4,678.1. Moreover, a newly designed rectangular plate with curved resonator body exhibits a very high *Q* of more 6,000 in the air when operating in its Width Extensional mode resonance at 166 MHz. In addition, a rectangular plate resonator with multiple Phononic Crystal strip tethers shows low insertion loss of -11.5 dB at 473.9 MHz with a *Q* of 2,722.5 in the air. This resonator is an excellent candidate as a tank circuit for MEMS-based oscillator. Simulated vibration modes and resonances of these rectangular plate resonators match closely with measurement results. Most importantly, a thin-film diamond has been employed as a part of the resonator structural layer to increase the overall effective acoustic velocity of the resonator with stacked piezoelectric-on-structural layer. The extracted acoustic velocity of the diamond up to 16,000 m/s has been demonstrated. All the simulation and measurement efforts of the piezoelectrically-transduced MEMS resonators provide tremendous values for the future design.

Second, high-*Q* piezoelectrically-transduced ZnO-on-SOI resonators have been implemented as a tank circuit for a frequency-reference oscillator. Two-port equivalent circuit model is developed to guide the oscillator design. A dual-frequency MEMS-based oscillator has been successfully demonstrated with unique ability to source out two oscillation frequencies by locking into the different vibrational mode of the Width Extensional mode resonator. As shown by the time-domain measurements, these oscillators generate a stable sinusoidal waveform with peak-to-peak amplitude of 4.6V at 259.5 MHz and 2.3V at 436.7 MHz, respectively. Meanwhile, the fundamental oscillation frequency and its harmonics can be easily observed in a measured frequency-domain spectrum. The phase noise performance is rigorously investigated with several sustaining amplifier designs. In order to fully take advantage of this technology, low-cost and customizable integration between MEMS resonator and IC chip is explored by employing a novel 3-D printed hybrid packaging approach.

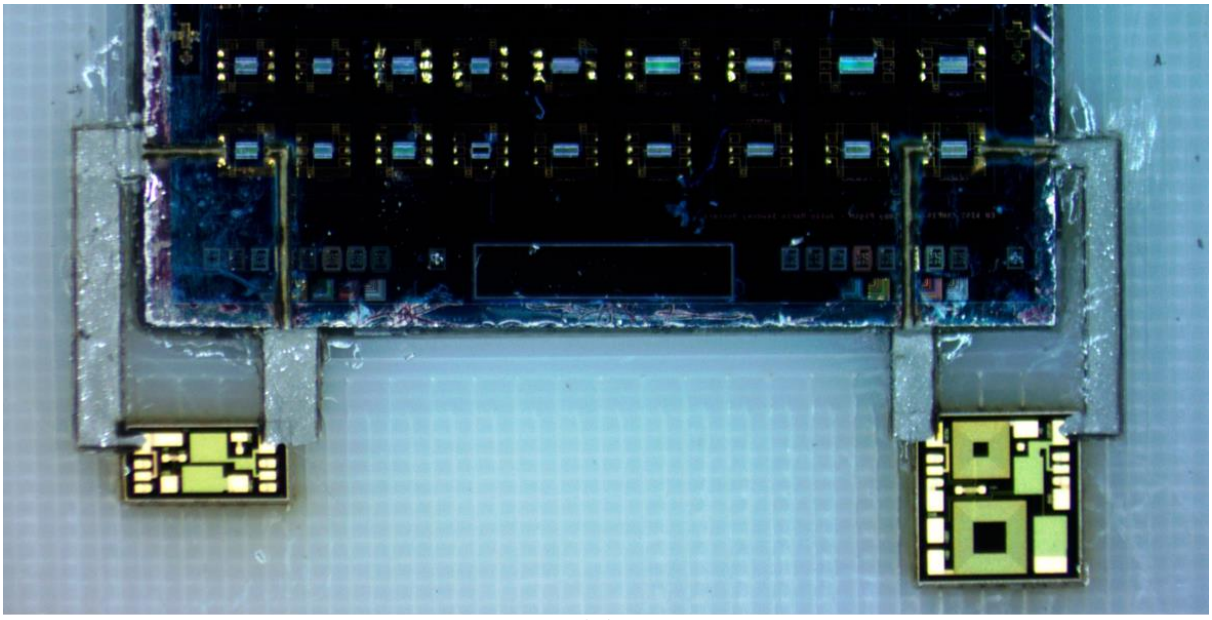
Third, a novel 3-D printed hybrid packaging that combines additive manufacturing and laser machining technique has been developed for hybrid integration of multiple functional IC chips for microwave and mm-wave applications. The fabrication process of this hybrid packaging has been well established through experiments. Particularly, two GaAs chips and one SMT component are successfully integrated into the proposed ABS package with sub-hundred μm lateral interconnects and sealed with an ABS encapsulation without any significant effects to the overall performance. The package is also evaluated in an environmental chamber and the frequency response of the microstrip line in the package suggests that Parylene N coating is needed to improve the resistance to water vapor (moisture). Besides the influence of the humidity level on the performance of the package, excessive heat or temperature increase can also lead to extra performance degradation. On-wafer probe measurements of a 50 Ω microstrip line on ABS

substrate ultimately exhibit its insertion loss of 0.028 dB/mm at 5 GHz, 0.187 dB/mm at 20 GHz and 0.512 dB/mm at 30 GHz, which include the effect of the prob pads at the input and output terminals, while showing satisfactory input and output return loss with the 3-D printed package. The intensive study of 3-D printed hybrid packaging reveals that the direct print additive manufacturing (DPAM) integration technology is very promising to be the next generation solution for system-in-package applications.

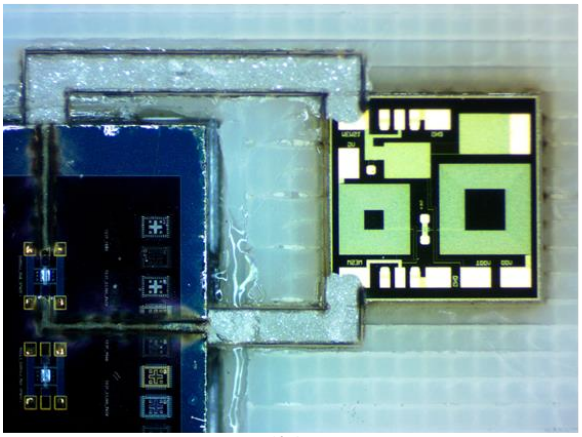
6.2 Future Work

Piezoelectrically-transduced ZnO-on-SOI resonators have proven themselves as an excellent candidate for single-chip multi-frequency applications. However, its performance hasn't reached its limitation yet. There is still more design room for the MEMS resonators to improve its performance even more. Beside single crystalline silicon, using high acoustic velocity nano-crystalline diamond (NCD) as the structural layer in the resonator body is explored in this dissertation, which have not been fully characterized and optimized. Electrode patterns can be further designed to match the vibration modes based on the FEM simulation model of the resonator developed in this work. Electrode material needs to be explored along with compatible fabrication processes. Meanwhile, the electrode thickness needs to be optimized for reducing the conductor losses.

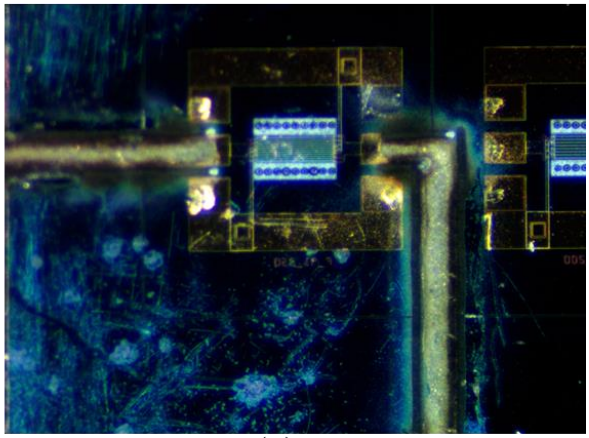
Based on the fundamental work of MEMS-based oscillator design done in this work, a variety of sustaining amplifiers designs can be further implemented and tested other than Pierce and Common-Emitter configurations.



(a)



(b)



(c)

Figure 6.1 – (a) MEMS-based GaAs oscillators in 3-D printed hybrid packaging; (b) a zoom-in view of an integrated MEMS-based GaAs oscillator using 3-D printing; (c) 3-D printed interconnects from the signal pads of a resonator

Even though ZnO piezoelectrically-transduced resonators on SOI wafer are integrated with GaAs sustaining amplifiers using 3-D printed hybrid packaging as shown in Figure 6.1 (a), more testing needs to be done in the future. Figure 6.1 (b) shows the zoom-in view of a MEMS-based oscillator with 3-D printed interconnects. Figure 6.1 (c) shows the zoom-in view of the interconnects from the resonator. An individual MEMS resonator needs to be separated from the rest so that the package can be miniaturized. Due to the co-existence of multiple IC chips from

different technologies in a single integrated package, the impedance of the 3-D printed interconnects requires more characterization and optimization for the future work.

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Thanks,

Di

APPENDIX B: DETAILED FABRICATION PROCESS FOR ZNO RESONATORS ON SILICON WAFER

Cleaning Samples
Label on the back of the wafer with Diamond Tipped Scribe
RCA clean
Solvent clean

1. Bottom Electrode (Mask Name: Bottom_Electrodes)

1.1. Lithography LOR10B and AZ1512

Equipment: Photoresist Spinner #1
- Spin LOR10B
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 4000 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180 °C

Equipment: Photoresist Spinner #1
- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=005 550

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner
- Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry

1.2. Descum

Equipment: March ICP O2 Plasma Asher
O2: 60 sccm
Pressure: 500 mTorr
RF Power: 70 W
Time: 2 min

1.3. Chrome Deposition

Equipment: AJA Sputtering
Power: 100 W RF
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 14 min (~40 nm)

1.4. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 18 min (~200 nm) Total 220 um measured

1.5. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and N_2 dry
Descum (**1.2**)

2. ZnO Deposition

Equipment: AJA Sputtering
Power: 100 W RF
O2: Ar 6:6 sccm
Pressure: 5 mTorr
Temperature: 300°C
Time: 5 hr (~550 nm)
Annealing: 300°C for 30 min, 600°C for 30 min

3. Open Vias Bottom Electrode (Mask Name: Vias)

3.1. Lithography AZ1512

Equipment: Photoresist Spinner #1

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=015 1650

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner

- Expose 7 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry

3.2. ZnO Wet Etch

Solution: 1: 100 = HCl: H2O (5 mL HCl, 500 mL H2O)
Submerge wafer in solution (5 min 40 sec for 550 nm ZnO, 6 min for 610 nm ZnO)
Rinse wafer with DI water
Solvent clean and N_2 dry

4. Top Electrode (Mask Name: Top_Electrodes)

4.1. Lithography LOR10B with G-Thinner (~LOR3B) and AZ1512

Equipment: Photoresist Spinner #1

- Spin LOR10B-G
  - Step 1: 10 sec @ 500 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3750 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180 °C

Equipment: Photoresist Spinner #1

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=0015 1650

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner
Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry
Descum(**1.2**)

4.2. Chromium Deposition

Equipment: AJA Sputtering
Power: 100 W RF
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 16 min (~30 nm)

4.3. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 11 min (~125 nm)

4.4. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and dry
Descum(**1.2**)

5. Pattern Resonator Body (Mask Name: Resonant_Body)

5.1. Lithography HDMS and AZ12XT

Equipment: Photoresist Spinner #1

- Spin HDMS
  - Step 1: 40 sec @ 3500 RPM, ACL=015 1650
- Spin AZ12XT
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3000 RPM, ACL=008 880
  - Step 1: 2 sec @ 6000 RPM, ACL=050 5500
  - Step 2: 10 sec @ 2000 RPM, ACL=008 880

Softbake: 2 min @ 110 °C

Equipment: EVG620 Mask Aligner
Expose 13 sec @ 9.7 mW/cm^2 with hard contact

Postbake 60 sec @ 90 °C
Develop 75 sec in AZ300
DI water rinse and N_2 dry
Descum(**1.2**)

5.2. ZnO DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
Ar: 16 sccm
CH4: 30 sccm
He: 8 sccm
Power: RF Source 1800 W / SH Biasing 200 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 1.3E-2 mBar
SH position from the source: 140 mm
Helium pressure: 10 mbar
Etch rate: ~100-120 nm/min
Time: 10 min for etching 550 nm of ZnO completely

6. Dry Release

6.1. SF6 Dry Etch

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
SF6: 300 sccm,
Power: RF Source 2000 W / SH Biasing 0 W
Pulsed power: 10 ms @ 5 W; 90 ms @ 0 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 0.1 mBar
SH position from the source: 160 mm
Helium pressure: 10 mbar
Etch rate: ~4-5 um/min (varies with opening size)

6.2. Photoresist Removing

Equipment: March ICP O2 Plasma Asher
O2: 60 sccm
Pressure: 500 mTorr
RF Power: 70 W
Time: 30 min

APPENDIX C: DETAILED FABRICATION PROCESS FOR ZNO RESONATORS ON SILICON-ON-INSULATOR WAFER

Cleaning Samples
Label on the back of the wafer with Diamond Tipped Scribe
RCA clean
Solvent clean

1. Pre-release (Mask Name: Holes)

1.1. Lithography HMDS and AZ12XT

Equipment: Photoresist Spinner #1
- Spin HDMS
  - Step 1: 40 sec @ 3500 RPM, ACL=015 1650

Equipment: Photoresist Spinner #1
Spin AZ12XT
- Step 1: 10 sec @ 300 RPM, ACL=015 1650
- Step 2: 30 sec @ 2000 RPM, ACL=008 880
- Step 2: 2 sec @ 6000 RPM, ACL=050 5500
- Step 2: 10 sec @ 2000 RPM, ACL=008 880

Softbake 80 sec @ 110 °C

Equipment: EVG620 Mask Aligner
Expose 13 sec @ 9.7 mW/cm^2 with hard contact

Postbake 60 sec @ 90°C
Develop 1min 20 sec in AZ300
DI water rinse and N_2 dry

1.2. Descum

Equipment: March ICP O2 Plasma Asher
O2: 60 sccm
Pressure: 500 mTorr
RF Power: 70 W
Time: 2 min

1.3. Si DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
SF6: 300 sccm, 3 sec
C4F8: 200 sccm, 1.4 sec; O_2: 20 sccm, 1.4 sec
Power: 1800 W
Base pressure: 7E-2 mBar
Pulsed power: 25 ms @ 100 W; 75 ms @ 0 W

Substrate temperature: -15 °C
Helium pressure: 13mbar
Etch rate: ~7 um/min

1.4. Thermal Oxide (Insulator, thickness = 2um) Wet Etch

Strip photoresist

Solution: 49% Hydrofluoric Acid (HF) + 3 drops of TritonX
Submerge wafer in solution for 30 min
Etch rate: ~5μm/min @ 25°C

Submerge wafer in methanol for 10 min
Submerge wafer in isopropanol for 10 min
Bake wafer in oven for 15 min at 110 °C

2. Bottom Electrode (Mask Name: Bottom_Electrodes)

2.1. Lithography LOR10B and AZ1512

Equipment: Photoresist Spinner #1

- Spin LOR10B
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 4000 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180 °C

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=005 550

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner
Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry
Descum (**1.2**)

2.2. Chrome Deposition

Equipment: AJA Sputtering
Power: 100 W RF
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 14 min (~40 nm)

2.3. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 18 min (~200 nm) Total 220um measured

2.4. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and dry
Descum (**1.2**)

3. ZnO Deposition

Equipment: AJA Sputtering
Power: 100 W RF
O2: Ar 6:6 sccm
Pressure: 5 mTorr
Temperature: 300 °C
Time: 5 hr (~550 nm)
Annealing: 300 °C for 30 min, 600 °C for 30 min

4. Open Vias Bottom Electrode (Mask Name: Vias)

4.1. Lithography AZ1512

Equipment: Photoresist Spinner #1

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=015 1650

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner
Expose 7 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry

4.2. ZnO Wet Etch

Solution: 1: 100 = HCl: H2O (5 mL HCl, 500 mL H2O)
Submerge wafer in solution (5 min 40 sec for 550 nm ZnO, 6 min for 610 nm ZnO)
Rinse wafer with DI water
Solvent clean and N_2 dry

5. Top Electrode (Mask Name: Top_Electrodes)

5.1. Lithography LOR10B with G-Thinner (~LOR3B) and AZ1512

Equipment: Photoresist Spinner #1

- Spin LOR10B-G
  - Step 1: 10 sec @ 500 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3750 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180 °C

Equipment: Photoresist Spinner #1

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=0015 1650

Softbake 50 sec @ 95 °C

Equipment: EVG620 Mask Aligner
Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry
Descum(**1.2**)

5.2. Chromium Deposition

Equipment: AJA Sputtering
Power: 100 W RF
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 16 min (~30 nm)

5.3. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 11 min (~125 nm)

5.4. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and N_2 dry
Descum (**1.2**)

6. Pattern Resonator Body (Mask Name: Resonant_Body)

6.1. Lithography HDMS and AZ12XT

Equipment: Photoresist Spinner #1

- Spin HDMS
  - Step 1: 40 sec @ 3500 RPM, ACL=015 1650
- Spin AZ12XT
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3000 RPM, ACL=008 880
  - Step 1: 2 sec @6000 RPM, ACL=050 5500
  - Step 2: 10 sec @ 2000 RPM, ACL=008 880

Softbake: 2 min @ 110 °C

Equipment: EVG620 Mask Aligner
Expose 13 sec @ 9.7 mW/cm^2 with hard contact

Postbake 60 sec @ 90 °C
Develop 75 sec in AZ300
DI water rinse and N_2 dry
Descum(**1.2**)

6.2. ZnO DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
Ar: 16 sccm
CH4: 30 sccm
He: 8 sccm
Power: RF Source 1800 W / SH Biasing 200 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 1.3E-2 mBar
SH position from the source: 140 mm
Helium pressure: 10 mbar
Etch rate: ~100-120 nm/min
Time: 10 min for etching 550 nm of ZnO completely

6.3. Si DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
SF6: 300 sccm, 3 sec
C4F8: 200 sccm, 1.4 sec; O_2: 20 sccm, 1.4 sec
Power: 1800 W
Base pressure: 7E-2 mBar
Pulsed power: 25 ms @ 100 W; 75 ms @ 0 W
Substrate temperature: -15 °C
Helium pressure: 13 mbar
Etch rate: ~7 um/min

APPENDIX D: DETAILED FABRICATION PROCESS FOR ZNO RESONATORS ON DIAMOND-ON-SILICON WAFER

Cleaning Samples
Label on the back of the wafer with Diamond Tipped Scribe
RCA clean
Solvent clean

1. Bottom Electrode (Mask Name: Bottom_Electrodes)

1.1. Lithography LOR10B and AZ1512 (~1.5um)

Equipment: Photoresist Spinner #1
- Spin LOR10B
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 4000 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180°C

Equipment: Photoresist Spinner #1
- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=005 550

Softbake 50 sec @ 95°C

Equipment: EVG620 Mask Aligner
Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105°C
Develop 25 sec in AZ726
DI water rinse and N_2 dry

1.2. Descum

Equipment: March ICP O2 Plasma Asher
O2: 60 sccm
Pressure: 500 mTorr
RF Power: 70 watts
Time: 2 min

1.3. Chrome Deposition

Equipment: AJA Sputtering
Power: 100 watts RF
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 14 min (~40 nm)

1.4. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 12 sccm
Time: 18 min (~200 nm) Total 220um measured

1.5. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and N_2 dry
Descum (**1.2**)

2. ZnO Deposition

Equipment: AJA Sputtering
Power: 100 W RF
O2: Ar 6:6 sccm
Pressure: 5 mTorr
Temperature: 300°C
Time: 5 hr (~550 nm)
Annealing: 300°C for 30 min, 600°C for 30 min

3. Open Vias (Mask Name: Vias)

3.1. Lithography AZ1512

Equipment: Photoresist Spinner #1

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=015 1650

Softbake 50 sec @ 95°C

Equipment: EVG620 Mask Aligner
Expose 7 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105°C
Develop 25 sec in AZ726
DI water rinse and N_2 dry

3.2. ZnO Wet Etch

Solution: 1: 100 = HCl: H2O (5 mL HCl, 500 mL H2O)
Submerge wafer in solution (etch rate: 250 nm-300 nm/min, i.e 500 nm ZnO, start with 2 min and etch every 10 sec more to achieve 1.8 um-2 um undercut)
Rinse wafer with water
Solvent clean and N_2 dry

4. Top Electrode (Mask Name: Top_Electrodes)

4.1. Lithography LOR10B with G-Thinner (~LOR3B) and AZ1512

Equipment: Photoresist Spinner #1

- Spin LOR10B-G
  - Step 1: 10 sec @ 500 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3750 RPM, ACL=015 1650

Softbake: 8 min 30 sec @ 180°C

- Spin AZ1512
  - Step 1: 10 sec @ 300 RPM, ACL=001 110
  - Step 2: 40 sec @ 2500 RPM, ACL=0015 1650

Softbake 50 sec @ 95°C

Equipment: EVG620 Mask Aligner
Expose 3.3 sec @ 9.7 mW/cm^2 with hard contact

Postbake 50 sec @ 105 °C
Develop 25 sec in AZ726
DI water rinse and N_2 dry
Descum (**1.2**)

4.2. Chromium Deposition

Equipment: AJA Sputtering
Power: 100 W RF
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 16 min (~30 nm)

4.3. Platinum Deposition

Equipment: AJA Sputtering
Power: 100 W DC
Pressure: 5 mTorr
Flow rate: Ar 6 sccm
Time: 11 min (~125 nm)

4.4. Lift-off

Submerge wafer in AZ400T for ~45 min @ ~60 °C
Rinse wafer with water
Solvent clean and N_2 dry
Descum(**1.2**)

5. Pattern Resonator Body (Mask Name: Resonant_Body)

5.1 PECVD SiO_2 (1.5 um)

5.2. Lithography HMDS and AZ12XT (~10 um)

Equipment: Photoresist Spinner #1

- Spin HMDS
  - Step 1: 40 sec @ 3500 RPM, ACL=015 1650
- Spin AZ12XT
  - Step 1: 10 sec @ 300 RPM, ACL=015 1650
  - Step 2: 30 sec @ 3000 RPM, ACL=008 880
  - Step 1: 2 sec @ 6000 RPM, ACL=050 5500
  - Step 2: 10 sec @ 2000 RPM, ACL=008 880

Softbake: 2 min @ 110°C

Equipment: EVG620 Mask Aligner
Expose 13 sec @ 9.7 mW/cm^2 with hard contact

Postbake 60 sec @ 90 °C
Develop 75 sec in AZ300
DI water rinse and N_2 dry
Descum (**1.2**)

5.3. SiO_2 DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
C_4F_8: 17 sccm
He: 150 sccm
CH_4: 13 sccm
Power: RF Source 1800 W / SH Biasing 400 W
Substrate temperature: -20 °C
Regulation mode: "postion 100%"
SH position from the source: 140 mm
Helium pressure: 13 mbar
Etch rate: ~400 nm/min
Time: 6-7 min for etching 1.5 um PECVD SiO_2 completely

5.4. ZnO DRIE

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
Ar: 16 sccm
CH4: 30 sccm
He: 8 sccm
Power: RF Source 1800 W / SH Biasing 200 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 1.3E-2 mBar
SH position from the source: 140 mm
Helium pressure: 10 mbar
Etch rate: ~100-120 nm/min
Time: 10 min for etching 550 nm of ZnO completely

5.5. Diamond DRIE

Equipment: Adixen AMS-100 Deep Relative Ion Etcher
O_2: 50 sccm
Power: RF Source 2800 W / SH Biasing 200 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 1.2E-2 mBar
SH position from the source: 140 mm
Helium pressure: 10 mbar
Etch rate: ~330 nm/min
Time: 30-40 min for etching 10um of diamond completely

6. Dry Release

6.1. SF6 Dry Etch

Equipment: Adixen AMS-100 Deep Reatice Ion Etcher
SF6: 300 sccm,
Power: RF Source 2000 W / SH Biasing 0 W
Pulsed power: 10 ms @ 5 W; 90 ms @ 0 W
Substrate temperature: +20 °C
Regulation mode: pressure
Base pressure: 0.1 mBar
SH position from the source: 160 mm
Helium pressure: 10 mbar
Etch rate: ~4-5 um/min (varies with opening size)

7. Residual SiO_2 Remove (5.3 2-3 min)

APPENDIX E: GAAS DISTRIBUTED LOW-NOISE AMPLIFIER DETAIL

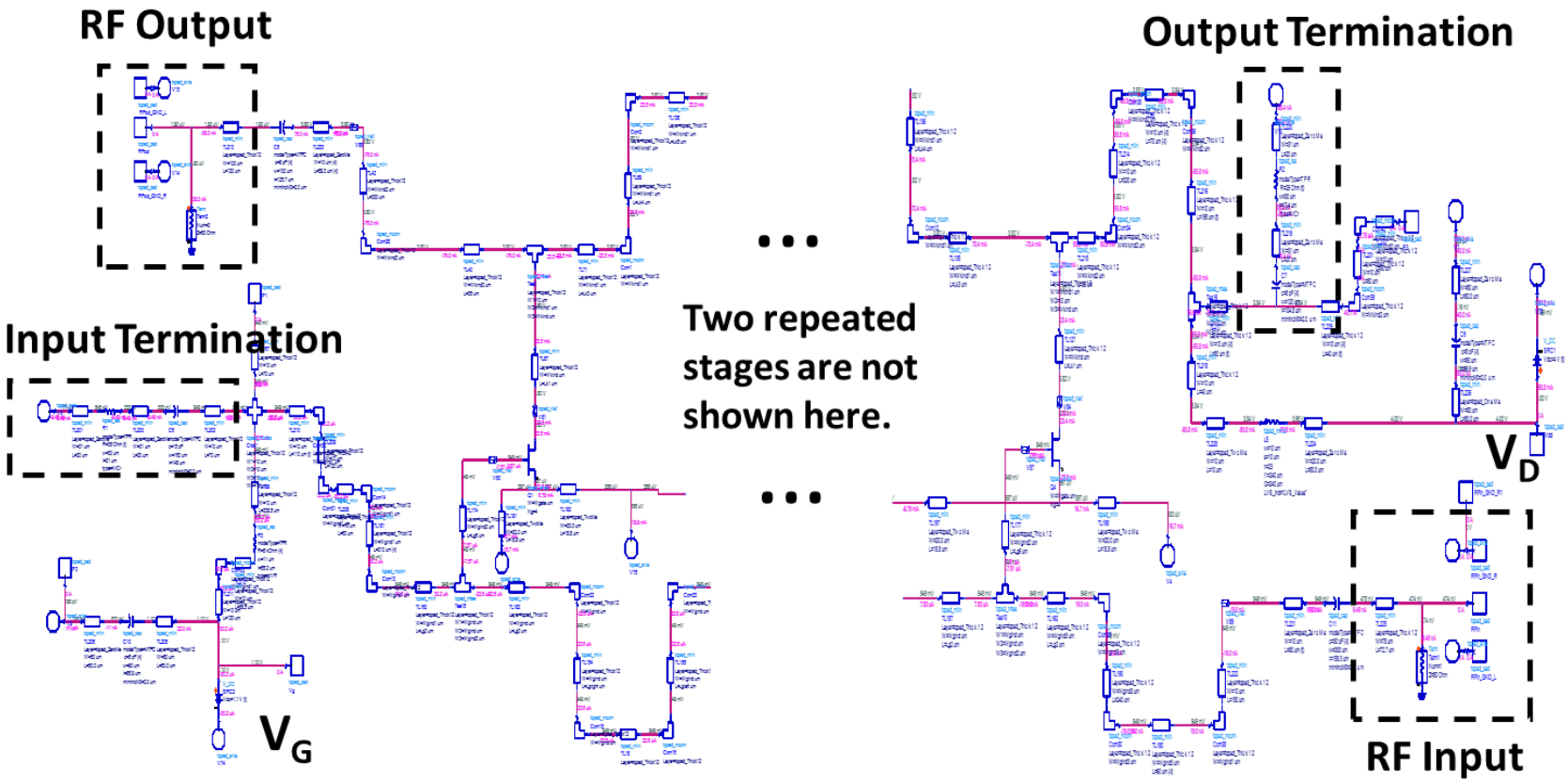

Figure E.1 – Schematic of a 4-stage distributed low-noise amplifier

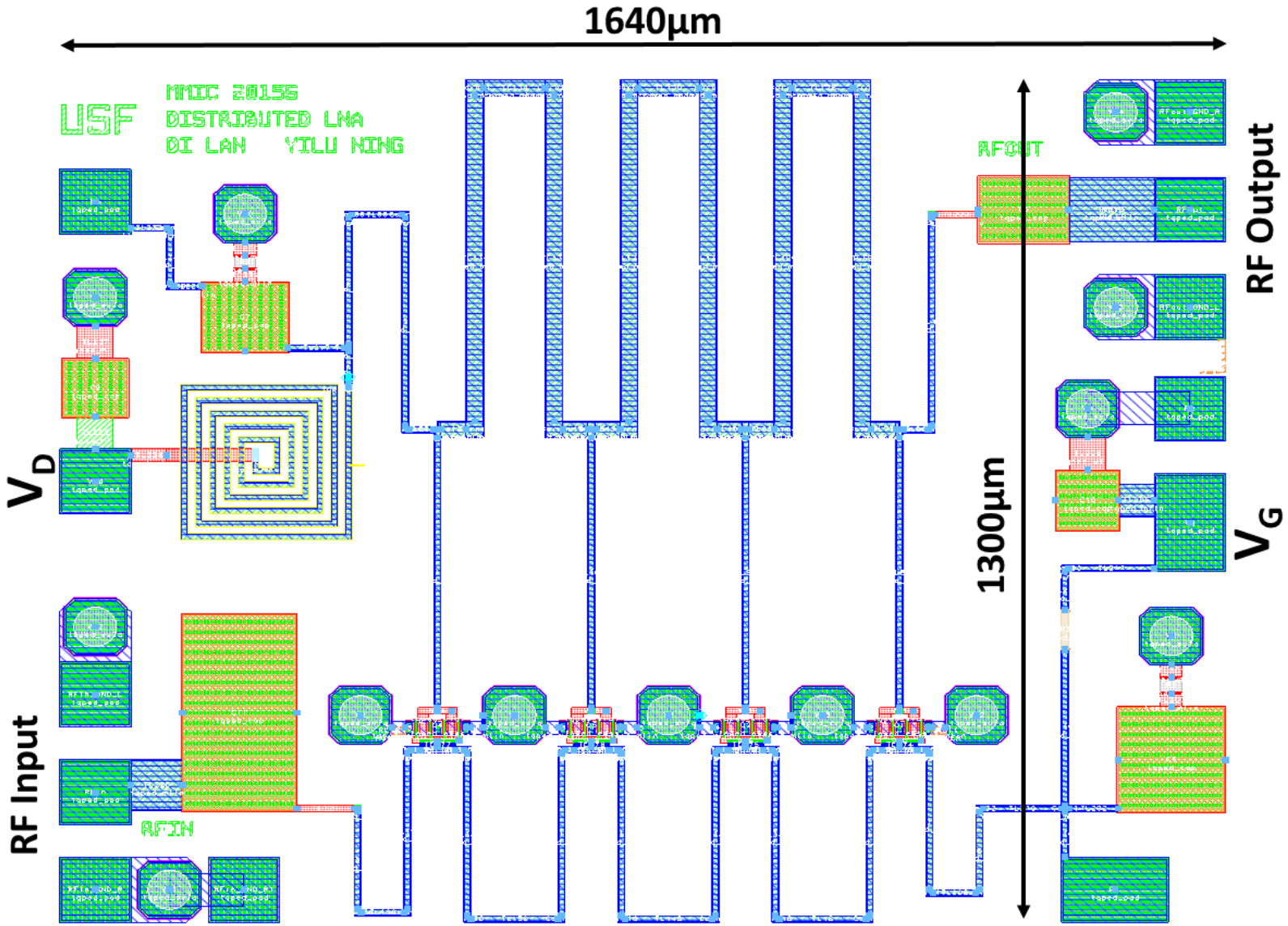

Figure E.2 – Layout of a 4-stage distributed low-noise amplifier

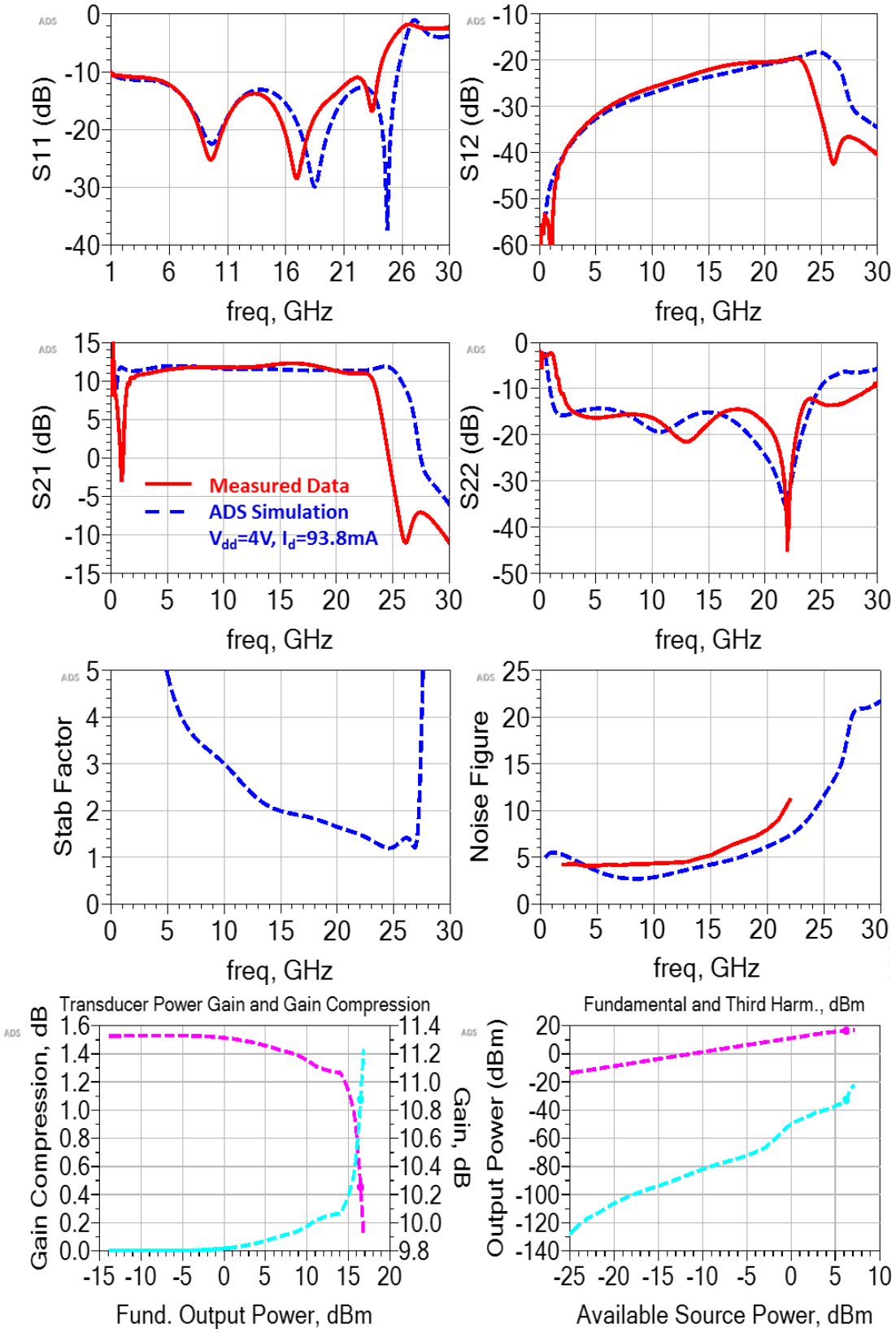

Figure E.3 – Measured and simulated results of 4-stage distributed low-noise amplifier

ABOUT THE AUTHOR

Di Lan received his BS and MS in Electrical Engineering from San Francisco State University (SFSU) in 2009 and 2012, respectively. Working in SF Bioelectronics Lab in SFSU, he had been involved in projects related to LC based MEMS passive sensor design and low-frequency wireless power transfer with AC/DC conversion for biomedical applications since 2008. He is currently working towards his Ph.D. in the RF MEMS Transducers Group. He is also a member of the WAMI Center in the Electrical Engineering Department at the University of South Florida (USF). His main research interests include RF integrated circuit design, MEMS resonator design , MEMS resonator fabrication, 3D-printing for RF/Microwave circuits and RF-products packaging.

Di was the recipient of the 2016 USF Dissertation Completion Fellowship. In addition, he received the USF 8th Annual College of Engineering Research Day Poster Winner Award in 2015. He was also the recipient of the USF Graduate Student Success Fellowship from 2012 to 2015.

Di worked as an RF Design Engineering Intern for Qorvo, Inc. during the summer of 2017, and worked as an RF Engineering Intern for Modelithics, Inc. from 2012-2016. Currently, he is an RF MEMS Engineer in II-VI, Inc.